Outlook for Advanced Semiconductor Process and Manufacturing Technologies

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OVERVIEW: Semiconductor manufacturers' particular emphasis is on providing LSI (large-scale integration) devices as best solutions in its lineup of microcomputer-based specialty products. This will involve not only performance and functionality, but an equal emphasis on holding down costs, achieving exceptional reliability, and minimizing time to market in developing new products. Supporting these efforts are semiconductor device technology and manufacturing equipment built by Hitachi Group, common technologies developed through national projects and consortiums, and high-reliability high-yield manufacturing technologies. By combining a silicon technology platform based on these manufacturing technologies and core technology-based devices, the Hitachi Group contributes to produce a wide range of specialty products and responds quickly to new user demands.

INTRODUCTION

PRODUCTION in the semiconductor industry fell sharply in the year 2001. Taking the market for DRAMs (dynamic random access memories) as an example, the market volume dropped to approximately a quarter of its peak volume (five trillion yen) in 1995[1]. There was no momentum toward recovery in 2002. Enormous structural changes have been taking place under these difficult circumstances as manufacturer oligopolies emerge and markets for the same product are divided up among many manufacturers.

However, now it is projected that we can expect to see a recovery from the latter half of 2003 due to gradually increasing demands for high-performance mobile equipment, digital home appliances, network systems, etc.

Specialty products such as used in cell phones, smart digital appliances, video games, etc. are in full production, and competitive products bolstered by superior technology are more important than ever. Given this climate, we are focusing our efforts on the creation of core technologies and deploying these technologies in products (see Fig. 1).

This article will highlight some of our initiatives in advanced semiconductor process and manufacturing technologies.

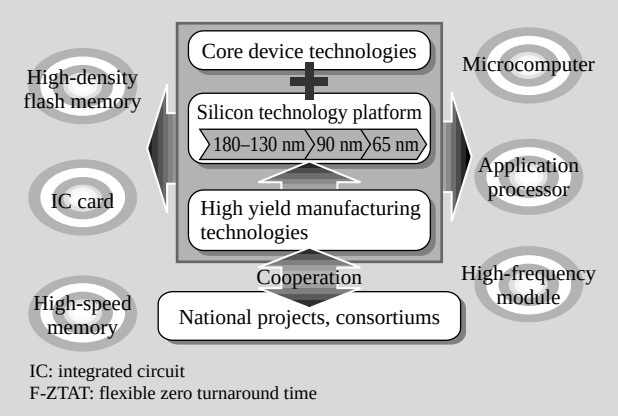


Fig. 1—Strategy of Core Device Technology.
Development of microcomputer-oriented high value added products based on a silicon technology platform and core device technologies.

ADVANCED MICROFABRICATION TECHNOLOGIES

CMOS Device Technologies

The basis of continued gains in performance and functionality of semiconductor and LSI devices is continued reduction of the feature size. We have developed a prototyping MOSFET (metal-oxide semiconductor field-effect transistor) with a gate electrode dimension of only 10 nm, and is now in the process of testing the device's operation and verifying the extent to which performance is improved at these reduced dimensions that will be required three generations from now[2] (see Fig. 2). In the process of developing the MOSFET—and as a perfect example of what we refer to as a core technology—we also developed a gate dielectric film that incorporates

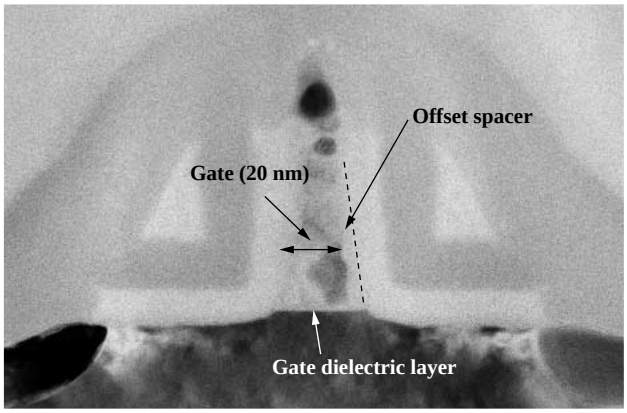


Fig. 2—Prototyping 20-nm-gate MOSFET.
SEM cross-sectional photograph of the preproduction MOSFET. The gate electrode is 20 nm (0.02 μm).

highly-concentrated nitrogen, and it was really this development that enabled us to achieve the extremely miniaturized MOSFET[3)].

The gate dielectric is of course a basic element of MOSFETs, and as the device evolves toward smaller features, the physical thickness of the film must also be thinned. The problem is that when the film thickness is reduced below 3 nm, tunnel leakage current flows between the gate electrode and the substrate, which hinders efforts to reduce the power consumption. Future generation devices will require gate dielectric film thicknesses of less than 1.5 nm, so finding ways to suppress this leakage current is an urgent priority. One practical solution is to incorporate nitrogen in the dielectric, and we have investigated methods of processing silicon oxide in nitrogen plasma. Incorporation of nitrogen effectively increases the dielectric constant of dielectric films, and this permits thinning of the electrical film thickness that affects MOSFET performance while ensuring adequate physical film thickness.

We have adopted a novel approach to the oxidation of nitride layers that is essentially different from past techniques. We achieved good success with a method that reduces nitrogen concentration at the interface between the gate oxide layer and the substrate (which has such an important impact on the performance of the MOSFET), while increasing the concentration of nitrogen in the oxide layer itself. Adopting this approach, we successfully developed a very thin gate dielectric film that is only 1.4 nm thick. We found that diffusion of boron from the p-type gate electrode to the substrate was effectively suppressed at the layer where nitrogen is highly concentrated, and this brought about the improvement in transistor performance.

High-density Flash Memory

We are starting to see the penetration of flash memory for data storage into everyday applications as a bridge medium between mobile devices and the home or office. The private network is one application that takes full advantage of the medium's mobility. For example, flash memory might be used to play back pictures taken with a digital camera and edited on a PC, or music or pictures downloaded from the Internet on a PDA (personal digital assistant) or even on a cell phone. Another potential application would be to use a PDA when away from the office on a business trip to verify corporate or financial data on a public network or customer data stored in flash memory.

Key issues are raised by this kind of flash memory: first off, the cost per bit must decrease as the density of the memory increases. One effective way to accomplish this would be to combine a multi-level cell (in which two bits' worth of data is stored in each memory cell) with smaller featured memory cells. Secondly, the write-programming speed must be increased. For example, in order to record one CD's worth of music (about 64 Mbytes in MP3 format) without stress in just a few seconds, it would require a throughput of 10 Mbytes per second, or roughly four times faster than the fastest throughputs available today.

We have now developed a 1-Gbit AG (assist-gate)-

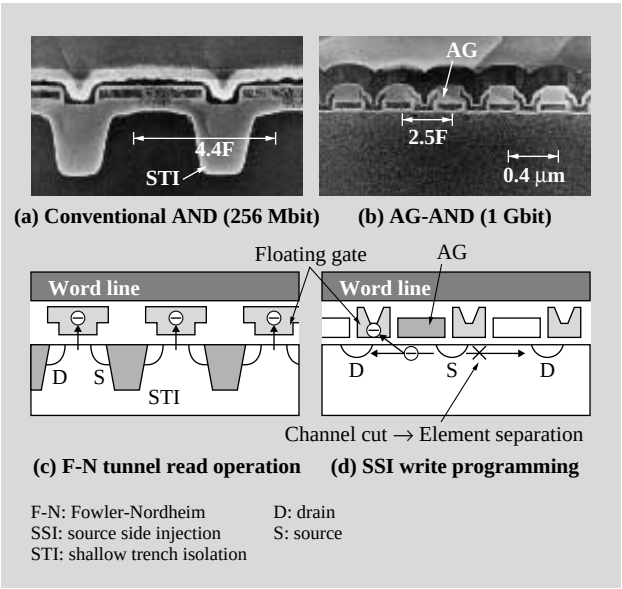


Fig. 3—Structure of the AG-AND Type Memory Cell.
This shows a comparison between the AG-AND type flash memory cell and the conventional AND-type cell. 4.4 F and 2.5 F are the feature sizes. In other words, the dimensions are 4.4 times F and 2.5 times F, respectively.

AND type flash memory device that achieves a very high write programming speed at low cost[4] (see Fig. 3). The new flash device features an original memory cell scheme in which AGs and floating gates are alternatively arranged to prevent interference between the memory cells. This also enables the cell area to be further reduced compared to the conventional approach of using STI to separate cells. To increase the write-programming speed, we replaced the conventional F-N tunnel injection with hot-electron injection. By using the AGs to perform hot- electron injection from the source, the injection efficiency into the floating gates is substantially improved, higher speed is attained, and parallel write-programming is achieved. Based on 130-nm process technology, a 1-Gbit device with the smallest chip area (95 mm^2) and a write-programming speed of 10 Mbyte/s was developed for the first time.

The flash memory technology will enable a host of flash memory card and system products and will provide even better cost efficiency and performance by applying 90-nm process technology.

Core Technology-based On-chip Memory Technology

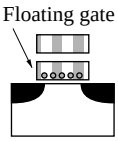
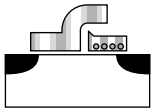
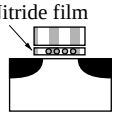
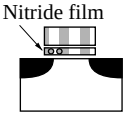
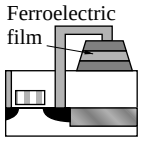
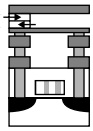
SoC (system-on-chip) technology is indispensable for achieving device multifunctionality, and certainly represents a core technology when nonvolatile memory is implemented on-chip. As shown in Fig. 4, there is a range of different types of nonvolatile memory, and which choice is best for a particular application will depend on how the device will be used, the required memory capacity, the cost, differences in technology for different companies, etc. A MONOS (metal-oxide-nitride-oxide silicon) type flash memory module with an ONO (oxide-nitride-oxide) film structure for the on-chip nonvolatile memory has been attracted much attention, and the device has already been implemented as a chip for IC cards and for SIM (subscriber identity module) cards[5]. For creative research and product implementation involving the MONOS type flash memory module, we received the 34th Industry Meritorious Achievement Prize of The Ichimura Prizes[6].

The MONOS type nonvolatile memory employs an ONO film structure—i.e., a nitride layer is sandwiched between two oxide layers—and data is memorized by storing charge in the nitride layer. This approach is fundamentally different from floating gate based memory cells, and because some charge is retained even when there are defects in the oxide layers, the nonvolatile memory provides excellent reliability. In the absence of floating gates, this design is also superior in terms of cost. Leveraging the excellent characteristics of the MONOS structure, new-type MONOS memory has been proposed, in which 2-bit/cell data storage is achieved[7].

HIGH-YIELD AND HIGH-RELIABILITY MANUFACTURING TECHNOLOGIES

Manufacturing Processes and Dimensional Variations

As gate dimensions continue to shrink, the importance of highly accurate fine processing technologies continues to grow at an accelerated pace. Optical lithography for the 90-nm technology node requires moving to a shorter exposure wavelength by switching from a KrF light source (λ = 248 nm) to an ArF light source (λ = 193 nm), and adoption of a scanner fitted with a very high NA (numerical aperture)

	Floating gate	Split gate	MONOS		FeRAM	MRAM	Phase change
			Entire injection	Local injection			
Memory method	Floating gate	Floating gate	Nitride film trap	Nitride film trap	Ferroelectric separation	Magnetic resistance effect	Phase change
Rewrite voltage	± 10 V	10 – 12 V	± 6 V	± 6 V	< 5 V	< 3 V	< 3 V
Number of rewrite times	-10^5	-10^5	$10^5 – 10^6$	-10^5	$10^{10} – 10^{12}$	-10^{16}	$10^{10} – 10^{12}$
Device structure (schematic)							

FeRAM: ferroelectric RAM
MRAM: magnetic RAM
TRM: tunneling magnetoresistive effect

Fig. 4—Comparison of Different Nonvolatile Memories.
Comparison of memory device characteristics that are likely to be used as on-chip flash memory for microcomputers is shown.

projection lens exceeding NA = 0.8.

To exploit the area near resolution limit, lacking sufficient contrast due to the optical proximity effect, a number of technologies are needed. Most notably are resolution enhancement technologies including a practical phase shift mask exposure method and an OPC (optical proximity effect correction) method, as well as technologies to improve pattern transfer accuracy.

Development work is also proceeding on an exposure tool and processing that uses shorter wavelength F2 light (λ = 157 nm), but this is clearly not going to be available for 90-nm node mass production, so it is necessary to extend the life of ArF exposure technology to cover the 90-nm node and beyond.

A major problem is that costs increase enormously for equipment using shorter wavelengths. For this reason, it is crucially important from the standpoint of maintaining product competitiveness to hold down manufacturing cost increase while at the same time working to minimize dimensional variations using more advanced process control technologies. As shown in Table 1, loss of dimensional accuracy can be caused by the exposure tool, by the process, or some other factors.

Particularly with the rapid increase of the MEF (mask error enhancement factor), even higher precision masks are critically important. The keys to achieve better OPC and better performance EB (electron beam) exposure systems are enhanced uniformity of mask in-plane dimensions, more accurate EBs capable of resolving fine patterns generated by OPC processing, and reduction of EB writing times—which has trade-off relationship with accuracy.

In another exposure-tool-related development we are seeing more extensive techniques to evaluate the lens aberrations available for users of techniques for evaluating the lens aberrations, which is helping reduce the amount of lens aberration. As it is insufficient to improve only lower-order aberration, further decreasing the amount of lens aberration up to and including higher-order aberration is inevitably required. We have entered upon an era when the quality of the aberration control technology has a direct influence on the quality of device performance. While reducing the aberration of exposure tools to a minimum, implementing better aberration control in line with various optical conditions and pattern transfer is also desirable.

Requirements for Manufacturing and Inspection Tools

Now that the target dimension accuracy has reached the nanometer level, the measurement variation component (a major factor in subsequent dimensional variation) can no longer be ignored. OPC technology requires a number of measurements of dimensions and profiles of individual patterns in order for this tool to produce good OPC rules and make valid evaluations. Turning to the production line where emphasis is on manufacturing efficiency, better inline control for identifying and eliminating the dimensional variation factors mentioned earlier is required.

To satisfy this growing demand for more precise dimension and shape control technology, more advanced functionality, higher speed, and improved automation, a number of new evaluation technologies must be introduced in addition to upgrading the performance of conventional inline CD-SEM (critical dimension scanning electron microscope). These newer approaches include AFM (atomic-force microscope) and non-destructive cross-sectional metrology tools (scatterometry).

With fab equipment that take full advantage of these new technologies running around the clock, it is most

TABLE 1. Factors Contributing to Deterioration of Dimensional Accuracy in Lithography. *Deterioration of accuracy can be caused by the exposure tool, the fabrication process, the mask, and other factors. Improvement in mask accuracy is especially important.*

	In shot	In wafer	Between wafers
Mask	Variation in mask dimensions	—	—
Exposure tool	Lens aberration Flare (lens, illumination system) Equipment accuracy (focus, stage synchronization)	Process condition Nonuniformity Flare (lens, illumination system) Accuracy (focus, stage synchronization)	Stability (exposure equipment, resist processing equipment)
Process	Optical proximity effect OPC correction error Resist pattern roughness Substrate flatness (including micro-steps)	Resist pattern roughness Substrate flatness (including micro-steps) Distribution of underlayer characteristics (thickness, optical characteristics)	Stability Change in resist sensitivity Change in processing atmosphere Variation of underlayer characteristics

important to adopt a single wafer management that permits much more comprehensive quality control than the conventional lot-by-lot management approach, and establish manufacturing methodology that actualizes wafer processing in the shortest possible TAT (turnaround time). A concerted effort is now underway to develop these key technologies:

(1) Fab-wide advanced process control with associating multiple progresses

Resist pattern dimension feedback control that automatically corrects lithography and etching processes, and feedforward control that uses the resist dimensions to control the amount of slimming in the etching process.

(2) Integrated measurement and single wafer control

Single wafer control is making good headway through the integration of lithography systems with scatterometry, overlay metrology, and other optical measurement tools. The scatterometry capability has now been verified through testing, and it is integrated into process optimization and fault detection technologies.

(3) Fast and accurate measurement of device patterns

High-speed multipoint measurement and profile measurement tools are needed to evaluate narrower process windows and optimize processes. Specific needs include the ability to measure 2D (two dimensional) device pattern shapes and the ability to manage inline cross-section device profiles. From the standpoint of controlling gate dimensions that directly affect device characteristics, a tool that is capable of quantitatively evaluating pattern edge roughness should be brought on line at the earliest possible date.

Finally, considering the enormous impact that dimensional variation has on device performance, achieving closer linkage between microfabrication and circuit design technologies and more robust design technologies are extremely important. At the same time, maintaining fab equipment in stable operating condition by managing operational information of fab line equipment and having a good monitoring on fluctuation factors in fab are also necessary.

Also important to enhance yields and achieve the highest level reliability is the need to integrate the management of data across a wide range of processes with fab-wide control to keep the equipment in constant optimum running condition.

Copper Interconnect Technology

Mass production of damascene copper products for the 130-nm technology node began in the latter half of 2001. With seven layers of metalization (five copper interconnect layers), a very fast signal transmission speed is achieved by using a low-k fluorine-doped silicon oxide layer [FSG (fluorinated silicate glass) that has a dielectric constant of 3.7] and silicon carbon nitride layer to minimize interlayer capacitance (see Fig. 5).

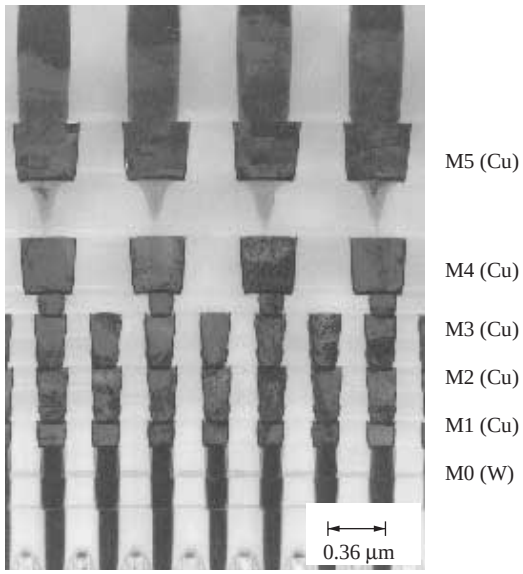


Fig. 5—Cross Section of Copper 5-Layer Interconnect for 130-nm Node.
Copper interconnects are processed using the dual damascene technology. Capacitance of the interconnects is reduced by using fluorine-doped silicon oxide (FSG has a dielectric constant of 3.7) and silicon carbon nitride (SiCN has a dielectric constant of 5) for the interlayer dielectric.

Copper processing is very different from aluminum processing in terms of the organization of the line and the process flow: new equipment including a self-ionization sputtering system and electroplating machine were used, a damascene process was adopted to form the interconnects, and other adjustments had to be made to adapt the processing for a 300-mm fab line. The major differences in making the conversion from 200-mm to 300-mm wafer processing were that (1) the adhesive strength was improved by using TEOS (tetraethyl orthosilicate silicon) as a constituent in FSG to prevent peeling of FSG at the edge of wafers, and (2) excellent flatness was achieved both locally and over the whole wafer by introducing non-selective polish slurry to prevent metal polish residue and polishing further to the interlayer dielectric during the metal polishing.

To reduce interconnect capacitance in next-generation devices and beyond, prevailing trends

indicate that SiOC (carbon-doped silicon oxide) will be used for the 90-nm technology node, while porous materials will be used for the 65-nm node after that. The tradeoff for moving to low-k materials is that these materials have insufficient mechanical strength and chemical resistance. For example, Young's modulus for these materials (i.e., an index of elasticity) is about one-fifth of silicon oxide film. This means that not only the adhesion strength at interfaces but also the strength of bulk itself is diminished, and this tends to further exacerbate problems such as peeling and scratching during copper polishing. It is thus necessary to reduce the polishing load while further improving the slurry material. One way to provide additional strength would be to simply introduce multilayer silicon dioxide, but the layer would cause the dielectric constant to increase. The process technology becomes more complicated when this kind of cap layer is used.

What is more, wire bonding pad delamination during packaging or other problems can occur due to the mechanical fragility of the interlayer film, so in designing an LSI device, careful consideration must be given to the entire manufacturing sequence including backend processing. It is currently very difficult to form all interlayer films using low-k material, and one sometimes observes upper layer copper interconnects being implemented using FSG or some other composite material.

Naturally, the insufficient chemical resistance of low-k materials also necessitates major changes to process flow and equipment specifications. For example, high-temperature oxygen plasma with wafer heating can not be used in the resist removal process. This is because the carbon in the low-k materials would be drawn out by the high temperature, thus causing the quality of the material to deteriorate. This deterioration is prevented by using oxygen plasma and reduction plasma under low temperature and pressure conditions. Some of the processes that must be designed with awareness of the relatively low chemical resistance include interlayer etching, via cleaning, deposition of cap layers on low-k material, and under some circumstances, appropriate surface processing must be applied.

We have seen that may very well be necessary to modify fab equipment and/or materials based on new concepts with each successive new generation of VLSI technology. Since this can involve enormous investment outlays for plant and equipment and long development cycles, the development of new equipment and processes is commonly undertaken by national institutes or consortiums.

DEVELOPMENT VERTICAL STARTUP TECHNOLOGY

QTAT Development

In order to respond quickly to fast-changing market needs, increasing the speed and reducing the cost of new product development are critically important. Speeding up the time it takes to develop products and ramp up to full production while maintaining stable quality productive yields is a fundamentally important factor in strengthening a company's competitive position in ULSI industry. Key points for minimizing the time to reach stable mass production are to analyze issues affecting device and process performance and to obtain feedback as quickly as possible during the preproduction stage (see Fig. 6).

Failure Analysis Technologies

Defects that occur in preproduction stage products are identified and corrected through a series steps:
(1) specify the defective circuit region through logic analysis,
(2) specify the defective region on the layout,
(3) specify the cause and propagating mechanism of the defect through physical analysis,
(4) specify the cause of the defect by analyzing the process history, and
(5) correct the process if necessary based on feedback from the analysis.

Note that although the first four steps call for specification, more often in actual practice this involves estimation in order to reduce the time required for the

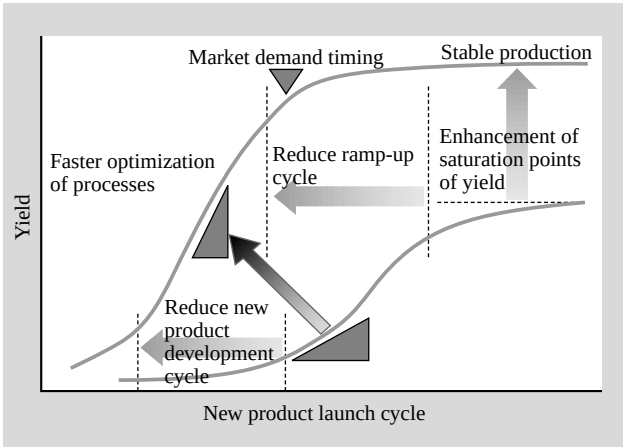


Fig. 6—Achieving QTAT is Essential to Reduce Time to Market. Quick analysis and feedback regarding problems that arise in the preproduction stage are critically important to achieve volume production that satisfies market requirements.

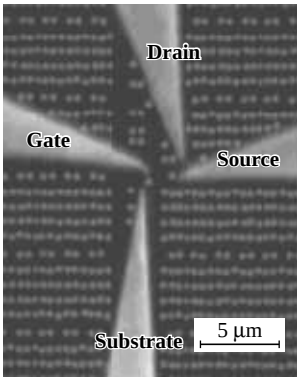


Fig. 7—Nano-prober Measurements.
The nano-prober consists of four submicron probes that evaluate the electrical characteristics of individual transistors in a chip.

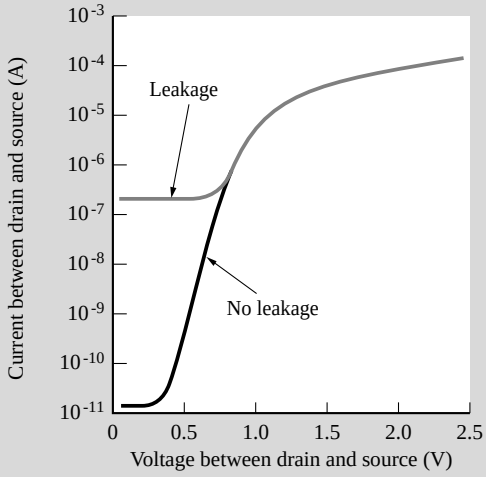


Fig. 8—Evaluation Results of MOS Transistors Characteristics.
Verification of leakage current associated with a contact in one of six MOS transistors configuring a failed SRAM.

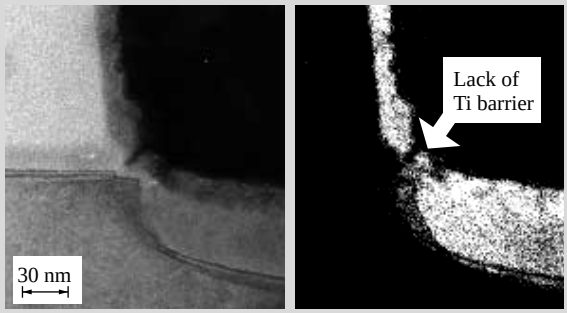


Fig. 9—Ti Barrier Analysis by TEM-EELS.
From the approximate structure at the bottom of the contact revealed by TEM cross section (a), and Ti elemental analysis (b), it is clear that the device is defective due to the non-uniformity of the Ti barrier layer, so the cause of the failure is specified.

defect analysis. Particularly for Step (1), we need a groundbreaking new technique to pin-point fault locations within a short time in order to develop ULSI devices for the 90-nm technology node and beyond. And to accurately analyze the mechanisms of faults in Step (3), we need techniques with better spatial resolution and analytical sensitivity than we have available today. To address these needs and achieve a QTAT (quick turnaround time), we are now developing a nano-prober[8] and a TEM-EELS (transmission electron microsope-electron energy loss spectroscopy)[9].

As shown in Fig. 7, the nano-prober has four submicron probes that evaluate the electrical properties of device elements when brought into contact with electrodes or interconnects. After narrowing down to a small number of candidate fault locations, the nano-prober measures the electrical characteristics of the sites to determine the exact location of the fault. This not only provides a clear picture of the structure of the fault location, it also provides a way of directly addressing the structural and electrical symptoms. TEM-EELS, on the other hand, exploits the resolution of TEM for elemental analysis and evaluates chemical bondings. The sensitivity of the system has been enhanced especially for application to IC device fault detection, and this tool provides a good way to closely analyze the fault regions detected by TEM and the mechanism causing the defect.

Figs. 8 and 9 show actual examples of how these tools are used in failure analysis. As shown in Fig. 8, the nano-prober measurement results clearly reveal that there is contact leakage in one of six MOSs (metal-oxide semiconductors) in a failed SRAM (static random access memory). Fig. 9 shows the Ti distribution in a cross section of the contact. It is apparent that a crack in the Ti barrier are causing tungsten encroachment which results in leakage. Based on this knowledge, the process was modified to provide better Ti coverage and this effectively eliminated the source of the defects. These fault analysis technologies not only contribute to a QTAT, they also prevent faults before they occur after full-scale production is under way.

The pace with which VLSI technology is evolving toward smaller features is relentless with 90-nm, 65-nm, and 45-nm technology nodes identified as the next three generations. Powerful inspection and analysis tools are obviously essential to support this ongoing miniaturization of device dimensions, and this

calls for an acceleration of development efforts and further technological breakthroughs.

CONCLUSIONS

This article described some of the core technology devices that we anticipate will emerge in the years ahead, and underscored the importance of built-in yield enhancement technology to control variations and ensure reliability, QTAT development, and defect analysis tools as process and manufacturing technologies that will support these future core technology-based devices.

By promoting a close linkage between the development of manufacturing equipment and the development of devices, we are committed to the early development and shipment of superior new semiconductor products. By leveraging the synergy achieved through the vertical integration of these manufacturing technologies, a silicon technology platform, and core technology-based devices, we are preeminent in providing best solution products tailored to the needs of our customers.

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