UHF-ECR Plasma Etching System for Gate Electrode Processing

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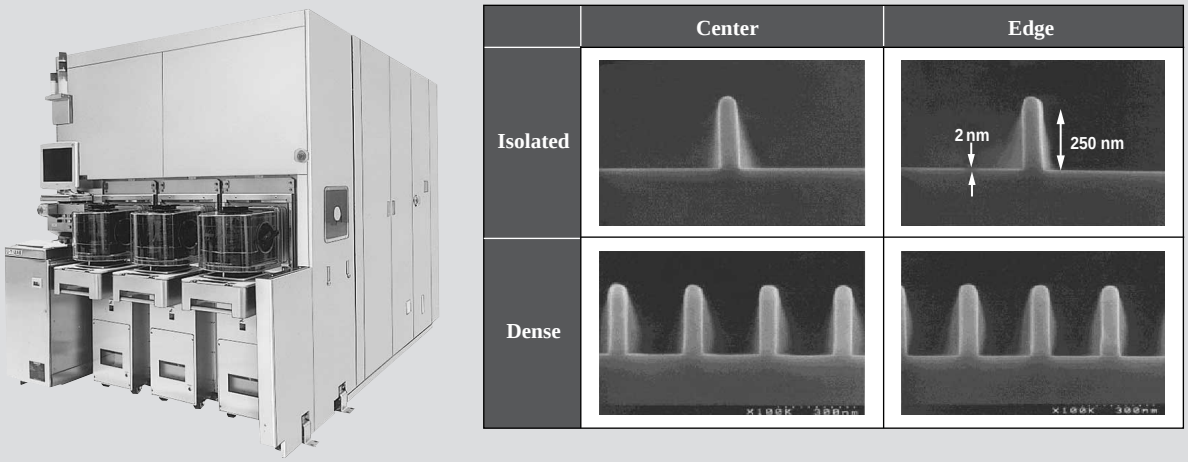
OVERVIEW: As the integration scale of semiconductor devices increases and the thickness of gate dielectric film decreases, fabrication without charging damage achieved through highly accurate CD (critical dimension) control is becoming important for gate etching systems. In addition, it is necessary to realize high uniformity across a 300-mm diameter wafer. To solve these problems, Hitachi developed a system that can perform highly accurate, low-damage etching by using UHF-ECR (ultra-high frequency electron cyclotron resonance) plasma to suppress the dissociation and deposition of reaction by-products (see Fig. 1). This system is capable of fabricating below 0.10-μm devices across a 300-mm diameter wafer. The system can also perform highly accurate fabrication without microtrenching, notching or other such deterioration of the etching profile, while maintaining high selectivity with respect to the underlying gate dielectric film. Good results are also being obtained in many other process applications in addition to poly-Si (polycrystalline silicon) gates, such as dual gates, polymetal gates and STI (shallow trench isolation). This system has the same base frame as the system that is already operating with high reliability on the mass production line, so stable mass production of devices is possible.

INTRODUCTION

UP to now, the mainstream method for gate etching has been to use a high-density plasma system, such as ICP (inductively coupled plasma) or microwave ECR (electron cyclotron resonance). However, the process margin for CD controllability and charging damage is becoming narrower, and there is a need to develop new systems that can cope with even further increases in



(a) Etching system

(b) Example of a 70-nm-wide poly-Si gate etching

Fig. 1—Etching System and Gate Electrode Etching Profiles.
The developed UHF-ECR plasma etching system (a) offers superior CD controllability that allows stable etching without profile variation across the wafer or between dense and isolated patterns (b).

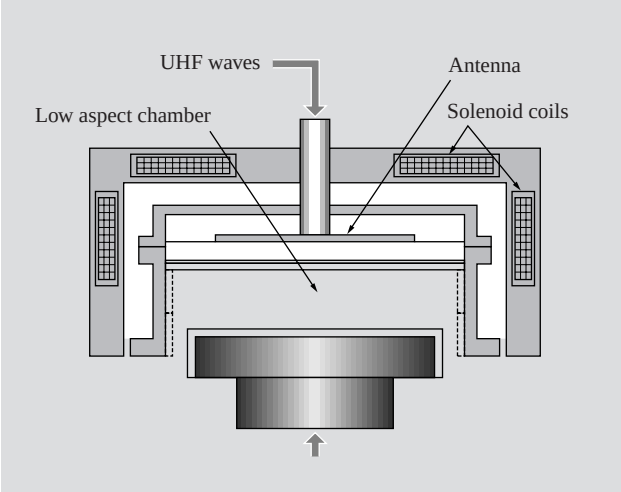


Fig. 2—Configuration of Etching Chamber Geometry.
The UHF waves produced by the antenna and the solenoid coils installed around the chamber generate a stable plasma.

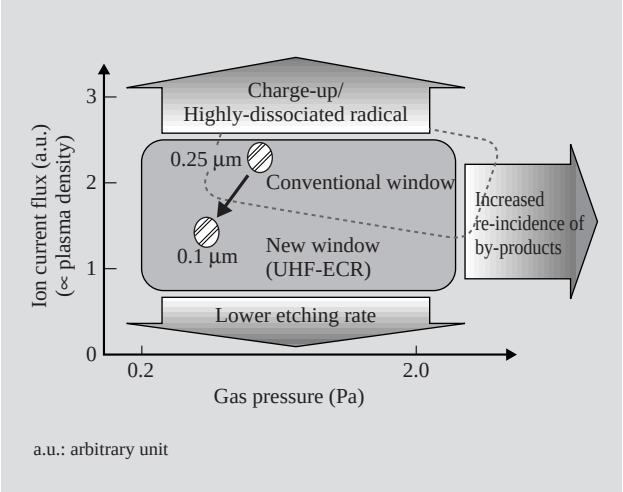


Fig. 3—UHF-ECR Plasma Generation Window.
The window is shifted to a region of lower pressure and more suitable plasma density compared to the window for the conventional microwave ECR methods.

integration scale in the future.

In October 1999, Hitachi produced a commercial dielectric etching system that can generate a stable plasma in the low pressure and medium- to high-density region by the UHF-ECR plasma technology. Judging that the UHF-ECR plasma is also suitable for solving these problems for gate etching, we also developed a UHF-ECR plasma etching system for gate fabrication.

As the integration scale of semiconductor devices increases, the requirements for etching are becoming more severe. In particular, the accurate fabrication of below 0.10-μm gates requires etching with high selectivity for extremely thin gate dielectrics with little variation in pattern density or etching profile across the wafer and little charging damage (damage caused by charging of photoresist or other insulation films on the wafer).

Here, we describe a UHF-ECR etching system that is capable of highly accurate, stable fabrication of gates on 300-mm diameter wafers.

PRINCIPLES AND FEATURES OF UHF-ECR PLASMA ETCHING

Configuration of the Etching Chamber

The UHF waves generated by the UHF power supply are introduced into the etching chamber via a coaxial cable and an antenna set on the atmosphere side of the quartz window. Solenoid coils are installed around the sides of the etching chamber, and a continuously stable plasma is generated in the low-pressure and medium-density region within a wide process window by the interaction of the UHF electric field and the magnetic field. The magnetic flux density for satisfying the ECR conditions of the UHF waves (450 MHz) is a weak 0.016 tesla (see Fig. 2).

Plasma Generation Technology for Gate Etching

The requirements for gate etching cover a wide range, including CD control, suppression of charging damage and high selectivity of the underlying oxide (dielectric) layer. Particularly important is suppression of the CD shift, which directly affects variance in the threshold voltage of transistor performance.

Furthermore, for devices in which the dense patterns of the memory cells and the isolated patterns of the logic cells coexist on the same wafer, such as in system LSIs (large-scale integrations), etching that produces little difference in the etching profiles of dense and isolated patterns is required.

The CD shift is increased when etching by-products that are desorbed from the wafer collide with etching-gas molecules near the wafer and adsorb on the side-walls of the gate patterns to form a deposit. Etching by-products are believed to strongly affect the difference between the etching profiles of isolated and dense patterns. Etching under low pressure conditions, where the frequency of gas collisions is lower, is advantageous for suppression of CD shifts and differences in profiles between dense and isolated patterns. On the other hand, if the plasma density is too high, the charge-up may cause device damage.

From these facts, we can conclude that the process window required for gate electrode fabrication should

be shifted to a region of lower pressure and more moderate plasma density. The developed system employs UHF-ECR to move from the previous process window to a new optimum window (see Fig. 3).

Highly Accurate Etching for Large-diameter Wafer Processes

To obtain high fabrication accuracy across the wafer, it is necessary to have a uniform plasma and etching gas distribution in the etching chamber so as to obtain a uniform distribution of etching by-products on the wafer.

The distributions of etching by-products for the UHF-ECR method and the conventional high-density plasma method are compared schematically in Fig. 4. With the conventional method, it is necessary to raise the height of the reaction chamber (the distance from the wafer surface to the top plate of the reaction chamber) to a certain degree to prevent charging damage. For that reason, the concentration of etching by-products is higher at the middle of the wafer, which easily results in a difference in CD shift across the wafer. The plasma generated by UHF-ECR, on the other hand, has a low electron temperature, which makes it possible to lower the height of the reaction chamber. Thus, by optimizing the supply of etching gas and the aspect ratio (ratio of height to inner diameter) of the reaction chamber, it is possible to control the etching gas distribution and make the distribution of deposited etching by-products uniform across the wafer. In that way, uniform process performance across the wafer can be obtained.

Furthermore, because high uniformity across the wafer and high fabrication accuracy can be achieved, an even higher accuracy across the wafer can be achieved, even in the fabrication of gate electrodes with multiple-layer structures.

SYSTEM CONFIGURATION

The base frame of this system is the same proven multiple-chamber system that is used in Hitachi's microwave (plasma) etching system. It has two etching chambers, and up to two ashing chambers can be added as options.

EXAMPLES OF ETCHING PERFORMANCE

Examples of UHF-ECR plasma etching performance for various gate materials are described in the following sections. To show the advantages of UHF-ECR plasma etching, data obtained from a 200-mm diameter wafer is used except as otherwise noted.

Example of Poly-Si Gate Etching

An example of an etched 70-nm poly-Si gate is shown in Fig. 5. The underlying gate oxide layer is 2-nm thick. We can see that vertical etching without microtrenching or notching profile abnormalities was achieved, while maintaining high selectivity with respect to the underlying gate oxide layer. CD variation of within 5 nm across the 200-mm diameter wafer was also achieved, with little CD bias between dense and isolated lines.

An example of the etching process for a 300-mm diameter wafer is shown in Fig. 6. Extension of the

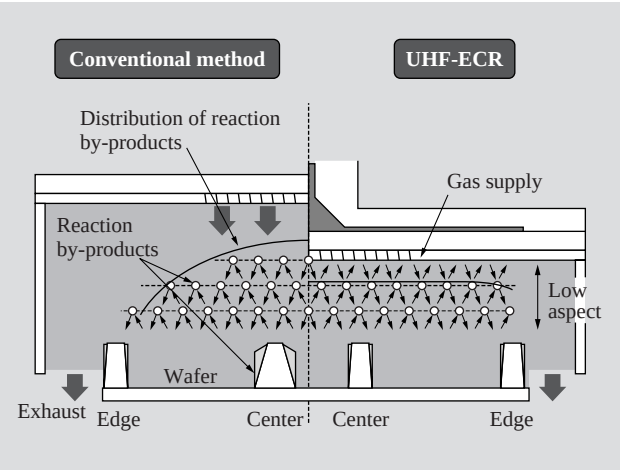


Fig. 4—Distribution of Reaction Products.
Reducing the reaction chamber height to create a low-aspect-ratio geometry makes it possible to achieve uniform process performances across the wafer.

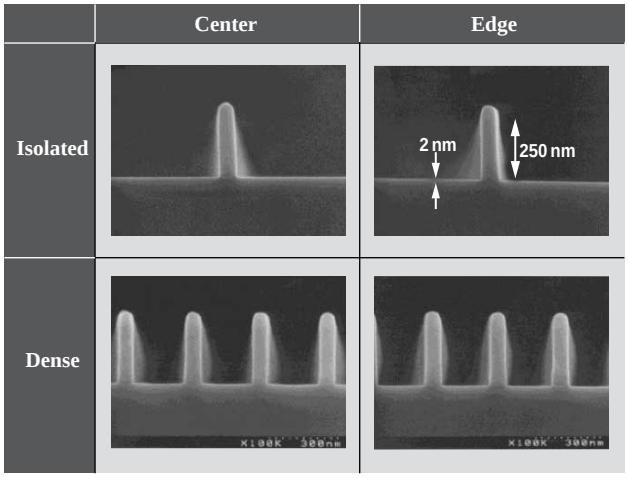


Fig. 5—Example of 70-nm Poly-Si Gate Etching.
Etching with little CD bias and without profile deterioration between the wafer center and edge or between dense and isolated patterns has been achieved.

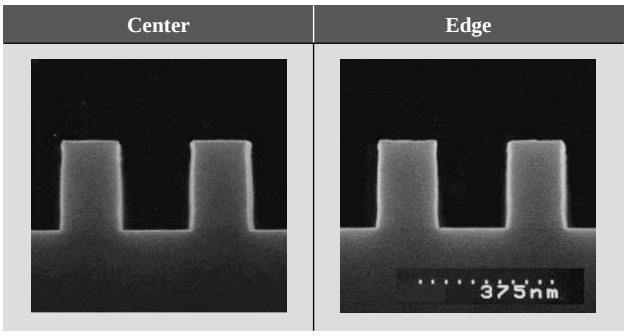


Fig. 6—Example of Etching on a 300-mm Diameter Wafer. Uniform and good process performances with little deterioration of the etching profile were obtained across the 300-mm diameter wafer.

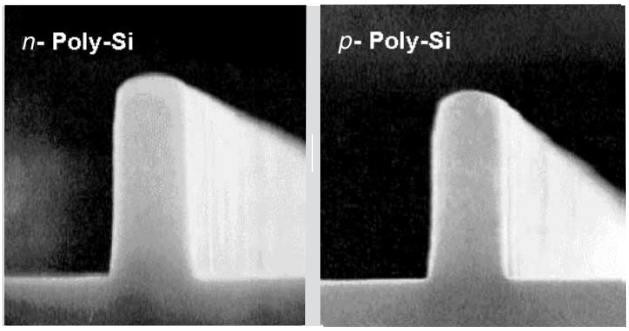


Fig. 7—Example of 80-nm Gate-length Etching. Etching profiles that were free from profile abnormalities such as microtrenching or notching and had little CD bias between p and n structures were obtained.

process from a 200-mm diameter wafer to a 300-mm diameter wafer was accomplished easily, and highly uniform process performances were obtained across the 300-mm diameter wafer.

Example of Dual Gate Etching

In dual gate etching, there must be little difference in process performances between p and n structures. Because the UHF-ECR plasma has a low electron temperature and the residence time of the gas in the low aspect ratio reaction chamber is short, excess dissociation of etching gas and etching by-products is suppressed. As a result, it is possible to reduce the differences in process characteristics between p and n structures.

An example of a dual gate etching process for an isolated pattern having a gate length of 80 nm is shown in Fig. 7. A hard mask is used, and the thickness of the underlying gate oxide is 3 nm. Anisotropic etching of a taper angle of 89 degrees or more was achieved without microtrenching or notching profile abnormalities. In this case, the mean CD shift difference between p and n structures was 4 nm.

FUTURE PLANS

Finer Processes

To achieve a dramatic improvement in CD controllability, it is necessary to further increase uniformity across the wafer, which is a feature of the UHF-ECR plasma method. We are also investigating the integration of a CD-SEM (scanning electron microscope) or an optical CD inspection device with the etching system to monitor changes in CD and improve controllability.

Improvement of Production Efficiency and Reduction of Cost

For improving productivity and reducing cost, the issues are improvement of OEE (overall equipment effectiveness) and reduction of consumables, including NPW (non-product wafers). For stable control of CD, we are investigating in situ equipment status management using APC (advanced process control), OES (optical emission spectroscopy) and other such means; for reduction of NPW and yield enhancement, we are investigating the introduction of in situ particle monitoring and other such means.

CONCLUSIONS

We have described various problems in the fabrication of gate electrodes and a method that employs UHF-ECR plasma to solve those problems.

The requirements placed on devices are steadily becoming more severe, and a further improvement of performance is needed. We believe that combining the UHF-ECR plasma method with peripheral technology is the way to continue to maintain top-class performance by control of the gate critical dimension.

Hitachi will continue efforts to increase performance up to the potential of the system and further develop the technology. We will also continue to contribute to the development of precise fabrication technology by actively making proposals.

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