Vertical SiGe Epitaxial Growth System

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OVERVIEW: The increasing sophistication of home electronics and telecommunication devices is propelling the demand for improved semiconductor devices. The SiGe (silicon germanium)-HBT (hetero-junction bipolar transistor) can realize high-speed operation, low noise, and low power consumption, therefore, its expected application to radio frequency IC communication devices is predicted to grow rapidly.[1)] SiGe can also be applied to strained-Si channels,[2,3)] which are responsible for the high performance of CMOS (complementary metal-oxide semiconductor)-LSIs (large-scale integrated circuits). SiGe-based devices are expected to be widely adopted, therefore, demand for a SiGe epitaxial growth system having high productivity is getting greater. In a timely response to this demand, Hitachi is moving forward with the development of an ultra-clean low-pressure CVD (chemical vapor deposition) vertical furnace for batch SiGe epitaxial growth. This batch-type vertical furnace system is able to process upto 50 wafers (200-mm diameter) at a time and it is capable of high-quality SiGe epitaxial growth at low temperatures (500°C) in an extremely clean ambient. A rapid ramp up/down heater has been adopted to reduce the heating and cooling times to acquire excellent crystallinity and high throughput.

INTRODUCTION

A base layer of SiGe-HBT is formed by continuously grading the Ge fraction in SiGe epitaxial film from zero to 10-25%. This graded structure creates a drift field in the base layer and leads to a drift acceleration of the electrons to move the HBT at high speeds. Conversely, in a single-wafer SiGe epitaxial growth system, which is widely used for epitaxial growth presently, it takes a long time to perform the epitaxial process, therefore, its processing capacity is low and COO (cost of ownership) is very high. For the mass-production of SiGe-based devices, a system that has a high process capacity and reduces COO is required. To meet these demands, we have developed VERTRON-V(SE), a vertical SiGe epitaxial growth system, which forms high quality film and also realizes high throughput and low COO. The system features, basic performance, results of an evaluation of this system, and the results of a gas flow simulation in a reactor are described below.

SYSTEM FEATURES

A photograph and the configuration of the vertical SiGe epitaxial growth system are shown in Figs. 1 and 2. The reactor and load lock chamber has been improved to realize ultra-clean ambient for low-temperature epitaxial growth, while most of the other

Fig. 1 — SiGe Epitaxial Growth System VERTRON-V (SE). The ultra-clean low-pressure CVD system for batch SiGe epitaxial growth, proposed by Hitachi Kokusai Electric Inc.

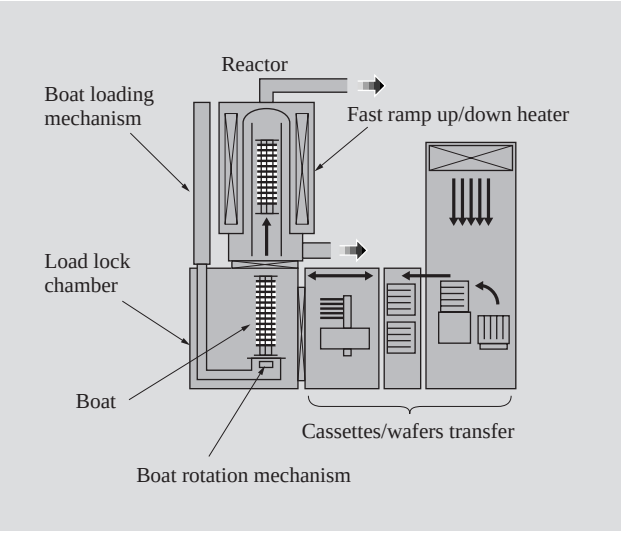

Fig. 2 — Configuration of Vertical SiGe Epitaxial Growth System.
Reactor and load lock chamber are improved to realize ultra-clean ambient. The transfer systems, for cassettes and wafers, etc. are standardized to conventional system.

parts are the same as those found in a standard LPCVD (low-pressure chemical vapor deposition) system.

Ultra-clean System

Roughness, misfit dislocations, and impurities (oxygen, etc.) at the epitaxial interface may cause deterioration of device performance. To realize a smooth surface at a high-Ge fraction condition, epitaxial growth should be performed at low temperatures around 500°C. To create a high-quality crystal at low temperatures, an extremely clean ambient is required to perform epitaxial growth.

We have worked on a gas flow modification in the reaction chamber to prevent contamination from reaching the process wafers. In addition, we optimized the load lock chamber to realize ultra-clean ambient. Commonly, the load lock chamber contains a boat rotation and loading mechanisms, which are potential contaminant sources. In this system, we modified its structure to isolate those mechanisms and electric wire/sensors from the load lock chamber.

Pre-cleaning of Wafer Surface

The process to realize a clean surface prior to SiGe epitaxial growth is as follows:

(1) Conduct a wet cleaning of the process wafers with diluted HF solution in advance to remove native oxide and enter those wafers into the system.

(2) After transferring wafers from the cassette onto a boat in a load lock chamber, the load lock chamber is evacuated and purged by nitrogen gas.

(3) Then load a boat into the reaction chamber at low temperature. Purge the reactor tube with high-purity hydrogen gas and raise the temperature in the reaction chamber to remove impurities on the wafer surfaces by thermal desorption.

(4) After conducting an hydrogen anneal to remove residual native oxide and contaminations, change the process temperature, and then start the epitaxial growth.

The above process leads to a clean condition of the resulting epi-layer/Si-substrate interface.

High Throughput

In the SiGe-HBT process, dopant concentration has to be controlled accurately and Ge fraction profile control is required to obtain a graded SiGe-base-layer formation. Consequently, as determined by a gas consumption efficiency calculation, the above requirements are satisfied by supplying sufficient Ge source gas into the reaction chamber by using one injection port and processing 50 wafers/batch. Furthermore, the use of a rapid ramp up/down heater to increase and decrease the temperature of the reaction chamber during a process and to reduce the ramp up/down time enhances the system's throughput.

Low COO

The conventional method used to create an extremely clean ambient in a batch-type furnace is to reduce the partial pressure of contamination by using the UHV (ultra-high vacuum) specification system configuration. On the contrary, instead of using the UHV specification, our system takes measures to maintain extreme cleanliness and adopts the medium vacuum region that is widely used in low-pressure CVD processes to realize a simple system configuration that is easy to maintain. Because of this, the system recovery time is reduced significantly. Also, the exhaust systems that are used for UHV, such as a turbo molecular pump or a cryo pump, are unnecessary. As a result, the cost of a system is reduced and a low COO is realized.

FLUID DYNAMIC ANALYSIS OF GAS FLOW

In a SiGe-HBT base layer growth process, steep concentration control for B (Boron) is required. We performed a fluid dynamic analysis of the gas flow to verify whether a batch-type furnace is able to control the dopant concentration steeply or not. The

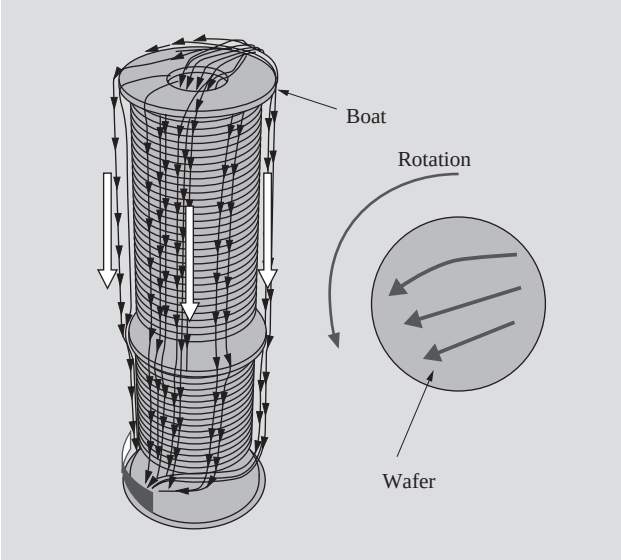

Fig. 3 — Result of Gas Flow Dynamic Analysis.
Analyzed under the condition of 500°C and 300 Pa. Gas flows around a boat and over wafers are not influenced by the boat rotation, and is similar to laminar flow.

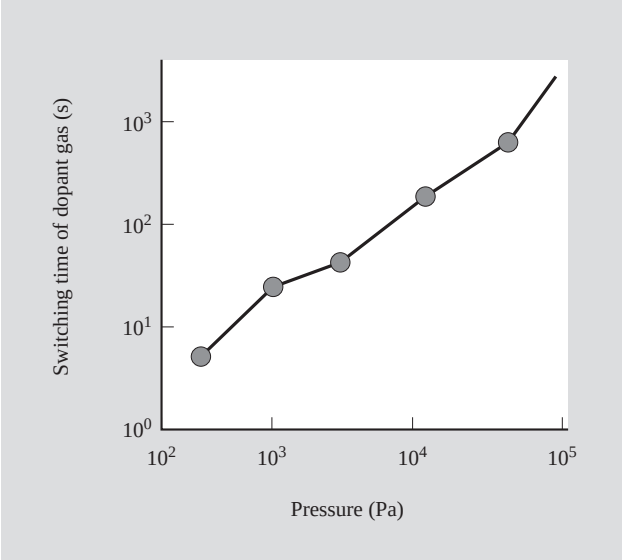

Fig. 4 — Dependence of Dopant Gas Switching Time on Growth Pressure.
Switching time of dopant gas depends on growth pressure. It can be reduced by lowering pressure.

temperature dependency of heat transfer, radiant heat, and gas properties, such as diffusion coefficients, viscosity, specific heat, and thermal conductivity, are considered to determine the temperature of gas or materials in the reactor.

The result of gas flow analysis is shown in Fig. 3.[4)] The gas flow is not influenced by a boat rotation. It is an almost laminar flow. On the contrary, the analysis indicated that boat rotation or convection affect the gas flow in a much higher pressure condition.

Fig. 4 shows the relationship between a switching time of doping gas and a pressure. As the figure shows, switching time strongly depends on the growth pressure, and rapid change is achieved at low growth pressures. At a pressure of 300 Pa it takes 5 seconds or shorter to switch the gas and the product of "switching time" and "growth rate" is as small as we can get the doping controllability in atomic scale. In other words, it is possible to conduct steep concentration control of B in a batch type furnace. In this analysis, no reaction of gas was considered. In the near future, we will perform an analysis of the reaction state.

BASIC PERFORMANCE AND PROCESS DATA

Table 1 shows the basic performance of the SiGe-HBT base layer growth process.

The following are the crystallinity evaluation data, graded-SiGe base-layer control data, and the oxygen concentration data in the hetero-interface:

(1) Epi crystallinity

An XTEM (cross-sectional transmission electron microscopy) photograph is shown in Fig. 5. The sample structure is a Si capping layer / SiGe film (Ge fraction = 0.3) / Si (100) substrate. Excellent SiGe epitaxial

TABLE 1 Basic Performance
Throughput is 16 wafers per hour in case of processing total 50 nm of simple Si/SiGe epitaxial structure. Remarkably improved throughput has been acquired compared to a single wafer-processing system.

Process temperature		450 - 550°C
Process pressure		> 30 Pa
Cleaning temperature (Removing native oxide)		< 750°C
Interfacial cleanliness (Oxygen)		< 2E12 atom/cm^2
Uniformity within wafer	Thickness	< +/- 2%
	Ge fraction	< +/- 2% (Ge fraction up to 30%)
	Boron concentration (Sheet resistance)	< +/- 3%
Particle (> 0.2 μm, transfer only)		< 10 pcs/wafer
Throughput (50-nm Si/SiGe epitaxial)		> 16 wafers/h

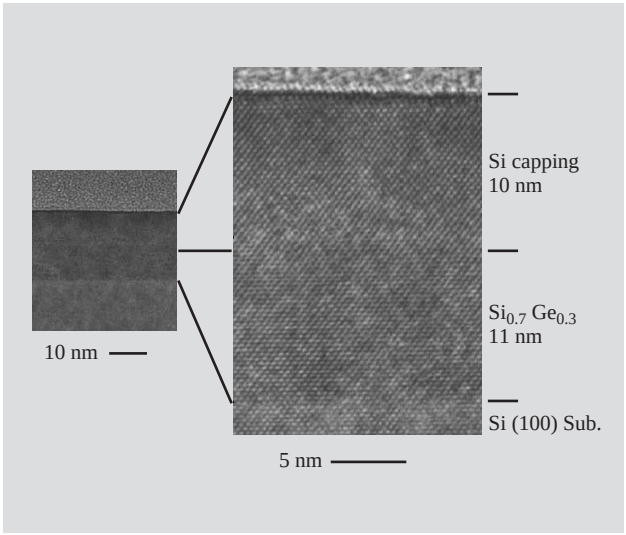

Fig. 5 — XTEM Photograph of Si/$Si_{0.7}$ $Ge_{0.3}$/Si Epi Structure. No misfit dislocations and smooth hetero-interface are observed.

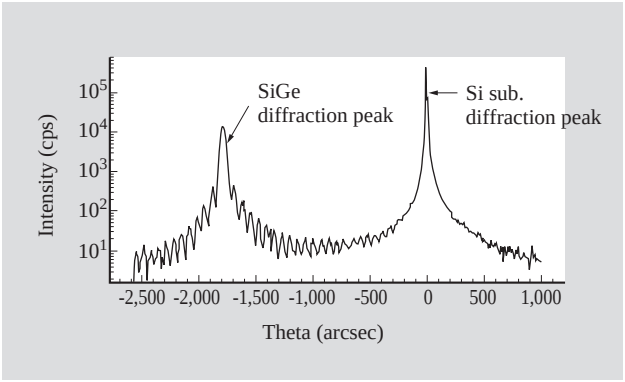

Fig. 6 — High-Resolution X-Ray Diffraction Data. The sample was a 300-nm thick SiGe epitaxial film with Ge fraction of 0.2 that was processed at 500°C.

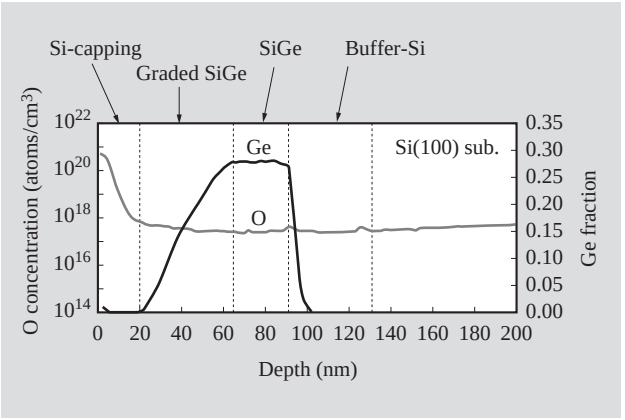

Fig. 7—SIMS Data of Epi Layers. SIMS data of sample with a buffer Si layer on Si(100) substrate, followed by SiGe layer with Ge fraction 0.3, SiGe layer with a Ge fraction graded from 0.3 to zero, and cap Si layer. Linear Ge graded fraction profile and no oxygen peaks at interfaces are observed.

crystallinity that contained no misfit dislocations and a smooth hetero-interface was acquired at the low growth temperature of 500°C.

(2) High-resolution XRD (X-ray diffraction) analysis

We used a high-resolution XRD to investigate the crystallinity of an epi-SiGe film (see Fig. 6). Sharp diffraction peaks with obvious intensity oscillation caused by interference indicate good crystallinity and smoothness of its surface and interface.

(3) Control of graded Ge fraction and concentration of oxygen in hetero-interface

Fig. 7 shows SIMS (secondary ion mass spectrometry) result. We confirmed that the graded Ge fraction was controlled accurately with a linear profile. High-quality epi layers that had no oxygen peaks at the interfaces of each layer were realized.

CONCLUSIONS

A vertical SiGe epitaxial growth system for mass-production of SiGe devices is described. This system performs epitaxial growth not only for SiGe-HBT but also for the type of strained-Si channel CMOS that researchers at Stanford University have developed, which device makers such as Hitachi have been promoting for practical use. In the future, we intend to expand its application by dealing with selective epitaxial growth for elevated source/drain CMOS. Development of this vertical system for batch SiGe epitaxial growth suggests the possibility of a definite role for vertical furnace in LSI processes beyond the 100-nm or 90-nm technology node.

It should be noted that there is a limit to the growth rate for forming high-quality films, such as a low-temperature SiGe epitaxial layer. Also there is a limit to the cycle time for switching gases to process ALD (atomic layer deposition). Therefore a batch-type furnace is expected to enhance its throughput. By exploring new concepts, such as an extremely clean ambient and ALD, we hope to succeed in developing a highly reliable process using hardware that has been devised in the long history of vertical furnaces. We believe that the batch-type furnace will allow the simultaneous realization of new device structures and a reduction of COO.

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