

Platform for System LSI Development

—“SOCplanner”: Reducing Time and Cost in Developing Systems—

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OVERVIEW: The SOC (system-on-a-chip) design methodology allows the configuration of whole systems from one or several chips in order to realize SIP (system in package) modules or MCMs (multi-chip modules). To design such chips, Hitachi has developed the “SOCplanner” system-on-a-chip platform for the quick implementation of hardware and software at low cost. The platform consists of libraries, design tools and design methodologies for effective system design.

INTRODUCTION

DEMANDS for performance improvements and reductions in power consumption, and shorter life cycles place a constant pressure on the production of electronic appliances. It is thus necessary to increase the ratio of software in such products and to accelerate the systematization of their production. Therefore, finding the optimum balance of hardware and software and co-verification of hardware and software are playing important roles in reducing the efforts involved in design.

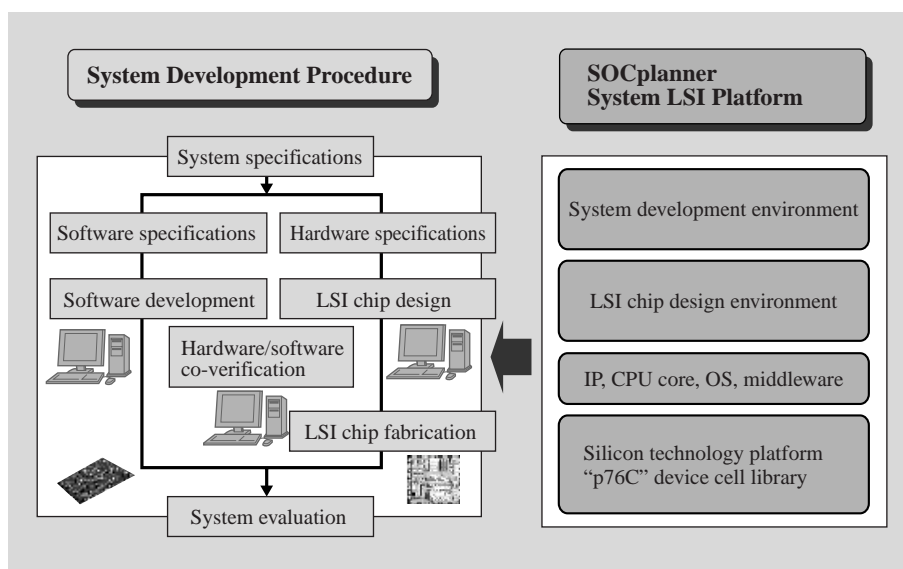
Deep-submicron technology has realized densities of several million gates and clock speeds in the several hundreds of megahertz. It has consequently become more difficult than ever for designers to efficiently develop and design large-scale, complicated, high-

speed products in short periods. Hitachi’s system-on-a-chip platform provides the solution to those problems.

OVERVIEW OF THE SYSTEM-ON-A-CHIP PLATFORM

This system-on-a-chip platform has four parts: (1) a system development environment, (2) an environment for designing LSI chips, (3) intellectual property (IP) cores, OS (operating system) and middleware, and (4) silicon-technology platform (see Fig. 1).

The system development environment (SDE) provides (1) high-performance software-development tools for developing systems in which Hitachi’s microcomputers are to be used, (2) a hardware/



SOC: system-on-a-chip
IP: intellectual property
CPU: central processing unit
OS: operating system

Fig. 1— The SOCplanner System LSI Platform from Hitachi. Hitachi provides a system-on-a-chip platform that consists of the libraries, design tools, and design methodologies to reduce the time required to develop complicated and large-scale systems.

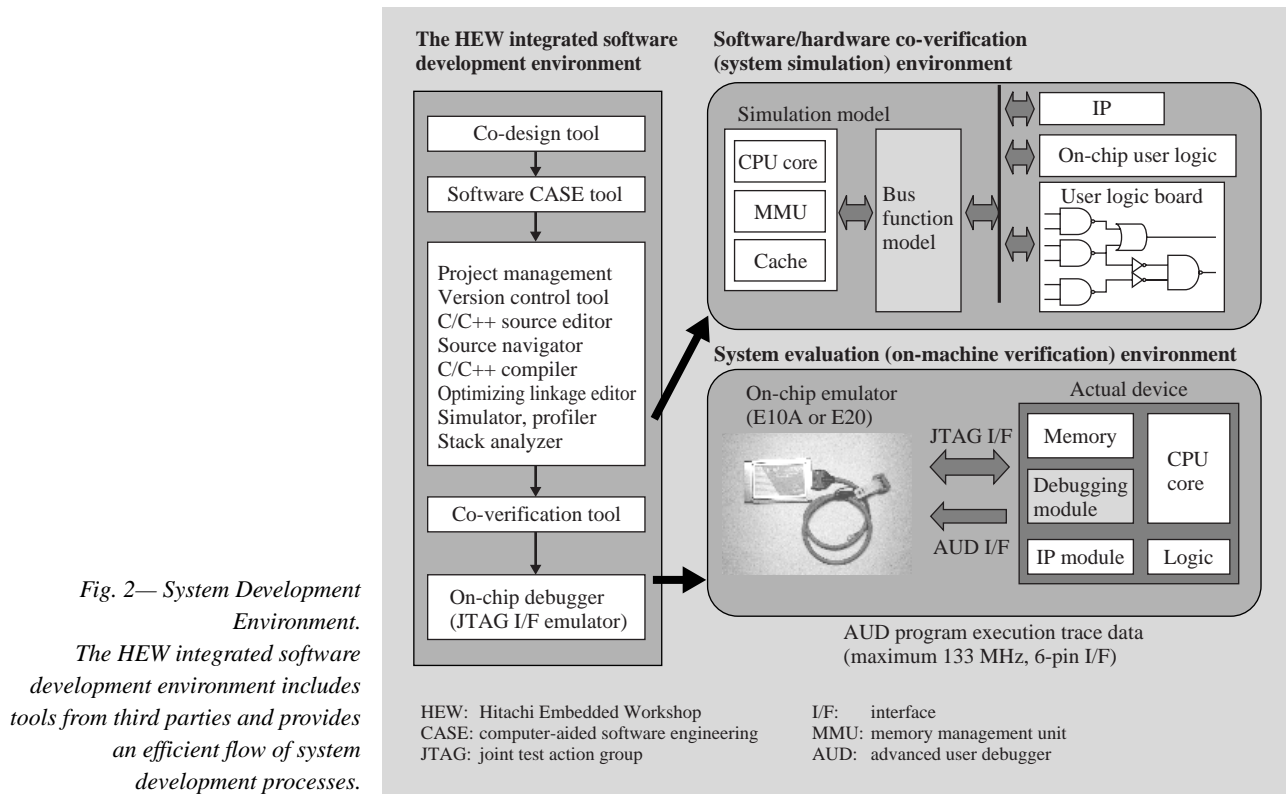


Fig. 2— System Development Environment.
The HEW integrated software development environment includes tools from third parties and provides an efficient flow of system development processes.

software co-verification environment and (3) an emulator (on-chip debugger) for evaluating systems.

The LSI design environment (LDE) provides design environment for a large-scale and high-speed system-on-a-chip and is built around a one-pass design concept, which avoids feedback from front-end to back-end portions of the design process.

It is necessary to re-use previous designs in order to more efficiently design large-scale systems. We provide the following IPs: CPU (central processing unit) cores (H-8 and SuperH series microcomputers), USB (universal serial bus), IEEE1394, and JPEG (joint photographic expert group), and A-D/D-A converter modules, and others. In the future, we will provide an even wider variety of IPs to fulfill the needs of further fields of application.

The p76C silicon-technology platform is a brand-new CMOS (complementary metal-oxide semiconductor) technology and it has greatly improved transistor densities, levels of power consumption, and operating frequencies over those of previous Hitachi products.

SYSTEM DEVELOPMENT ENVIRONMENT

For designers involved in system development, both LSI hardware technology and the development

environment are important factors that influence system development periods. Hitachi provides environments that are available to operate in the early stages of system design, and this allows the setting up of development environments that are useful to designers. Fig. 2 shows the system development environment and development tools.

Software/Hardware Co-Design Environment

A simulation model of each CPU core is written in the C language. This is necessary for system design and evaluation, and for co-verification of software and hardware in front-end processes, and enables the use of co-design and co-verification tools available from EDA (electronic design automation) vendors. After logic design for the LSI chip is complete, the user logic, in the form of an FPGA (field programmable gate array), and the in-circuit emulator provided for the standard core make it possible for users to construct a system evaluation environment before the LSI chip is completed. Since the CPU core has an on-chip debugging function, the E10A on-chip debugger, available through the JTAG (joint test action group) allows debugging of the system by real-time emulation. The high-performance E8000 emulator is also readily available, and allows real-time tracing of

external buses running at up to 100 MHz.

Integrated Software Development Environment

The Hitachi Embedded Workshop, abbreviated as HEW, is a highly operable integrated environment for software development that covers the whole software-development process, from software-project management to system evaluation. This environment combines point tools such as C/C++, an optimization linker, profiler, simulator, debugger, source navigator, and evaluation board, and is based on a consistent concept.

LSI DESIGN ENVIRONMENT (LDE)

Timing convergence, low power consumption, and design for testing are all critical issues in realizing large-scale and high-speed deep sub-micron LSI chip designs. One-pass design is applied to realize timing convergence in the LSI (see Fig. 3). Design guidelines that lead to high-quality design are provided. The RTL (register-transfer level) floorplan, makes logic synthesis on the basis of the floorplan. It is thus possible to estimate power consumption at the RTL. Tools for formal verification, STA (static timing analysis), and estimating power consumption in the logic design stage are all provided. For test design, a high degree of fault coverage is realized, and many methods of design-for-testability (DFT) are provided. The wiring delays can be estimated in the logic design

stage by using the floorplan, and timing-driven layout makes it easy to obtain timing convergence. Without these methods, it is difficult to accurately estimate wiring delays before the layout stage, so the logic sometimes has to be modified after layout. The timing-driven layout makes the feedforward control of timing convergence possible and prevents such design feedback. The combination of this timing-driven layout and the RTL floorplan contributes to increase design productivity. For use with deep-submicron processes, Hitachi has developed tools for analyzing IR drops (voltage drops due to wire resistances) and verifying sufficiently low levels of crosstalk (electromagnetic noise induced in wires by the signals on other wires).

Hitachi has implemented an educational training program, to help users to obtain a thorough understanding of the approaches and methods involved.

IP AND SOFTWARE FOR REALIZING SYSTEM-ON-A-CHIP

The key to success in developing a large-scale system-on-a-chip with several million gates is to reuse IPs that have already been developed, verified, and used on many previous designs.

Hitachi has applied the following basic technologies to the design and development of a variety of reusable IPs:

(1) a standardized IP design methodology, independent

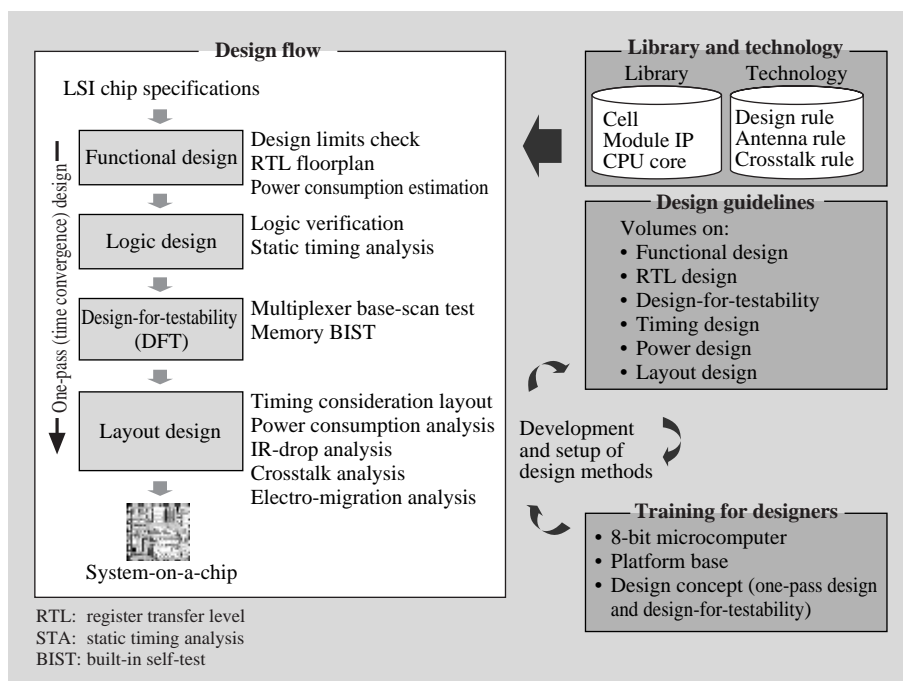


Fig. 3— LSI Chip Design Environment.

One-pass design flow, design guidelines and system-on-a-chip design training realize efficient LSI chip design environments.

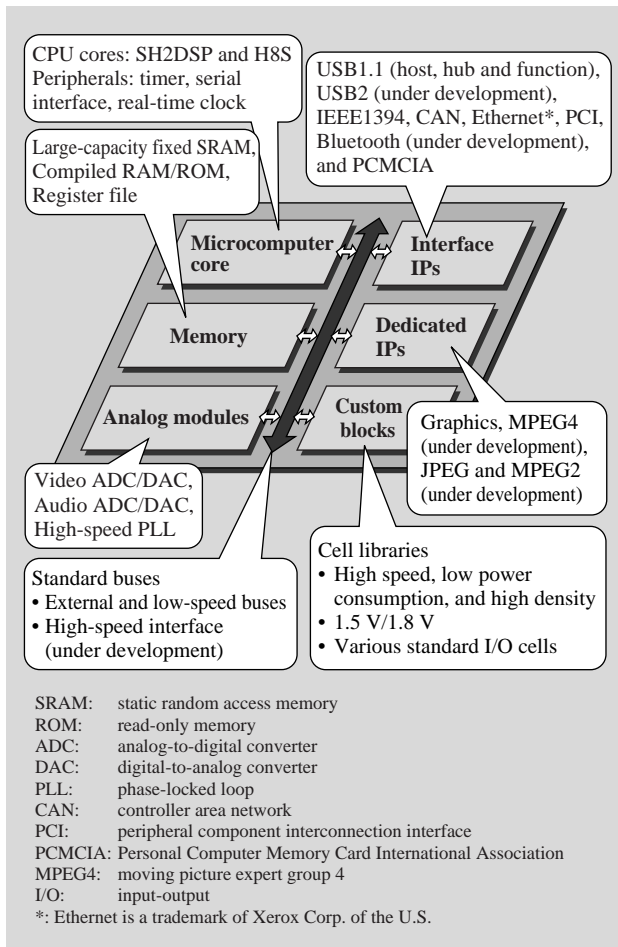


Fig. 4—IPs and System-on-a-Chip.

Various IPs help to improve efficiency in developing system-on-a-chip.

- of the semiconductor process technology;
- (2) IP socketization facilitating the combination of various IPs; and
- (3) an efficient IP management and distribution system.

Some of the IPs to which Hitachi has applied these standard design and management/distribution methods are shown in Fig. 4. Hitachi has also promoted the development of a variety of software for controlling system-on-a-chip that consist of combinations of above IPs (see Fig. 5).

Reusable IPs, preinstalled OSs and middleware enable the efficient development of system-on-a-chip for various applications.

THE p76C SILICON TECHNOLOGY PLATFORM

Fig. 6 gives an overview of Hitachi's silicon technology platforms, placing the p76C in context. One major feature of the p76C platform is that it allows designers to realize their various needs by combining

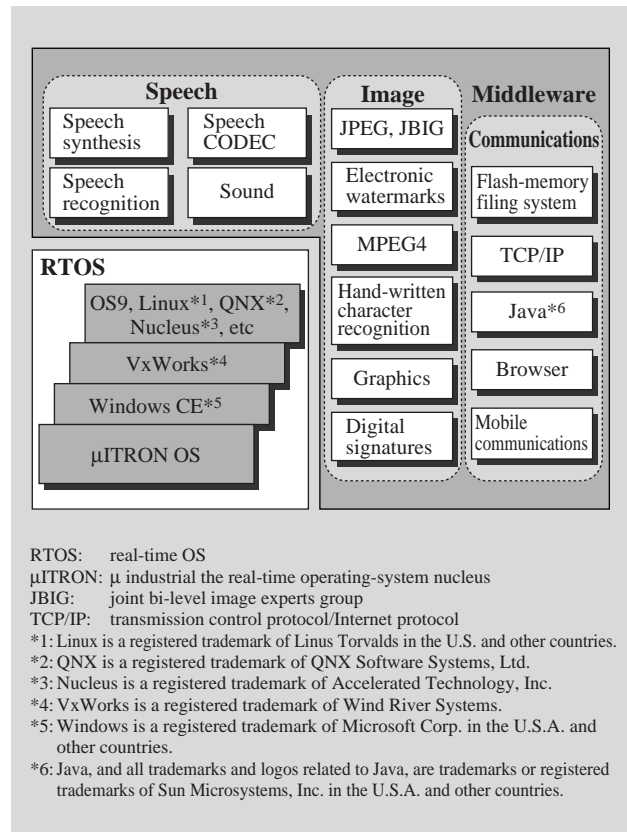


Fig. 5—Middleware and Preinstalled OSs.

Hitachi provides standard real-time OSs and a variety of middleware for communications and speech, and processing of images, etc.

various systems on a single chip, including the high-performance SuperH series microcomputers, analog-digital-hybrid circuits, and so on.

Hitachi has already used 0.18- μm technologies to develop a new cell library, as the basis of our system-on-a-chip platforms. In view of the various fields of potential application, we have developed logic cell libraries for high-speed LSIs and for high-density and low-power LSIs, as well as the standard p76C logic cells that operate with power supplies of 1.5 V and 1.8 V. Hitachi also provides compiled memories that allow the flexible design of word-bit configurations to suit users' applications and specifications, memory modules with large capacities of more than 1 Mbits, and a variety of analog modules for use as hardware cores.

The CMOS-device process technology that we are using in the p76C platform has gate lengths of 0.14 μm , a metal pitch of 0.52 μm and up to 5 metal layers.

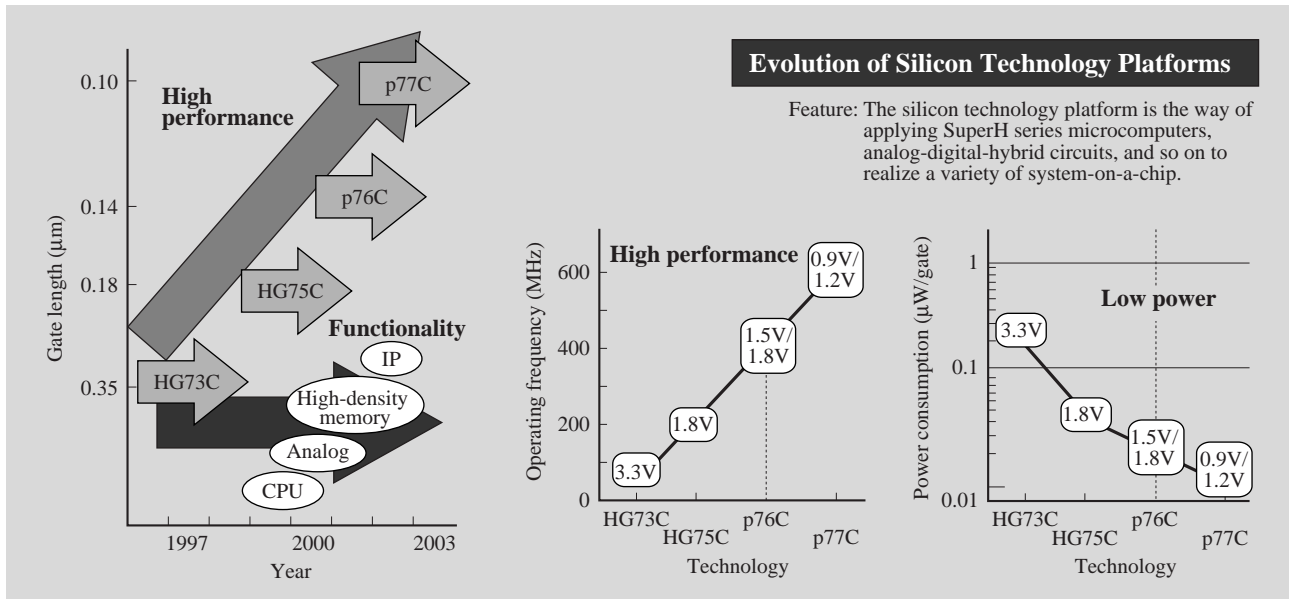


Fig. 6—Silicon Technology Platform.

State-of-the-art CMOS hardware technology has realized high-performance, low-power consumption system-on-a-chip.

CONCLUSIONS

We have introduced Hitachi's SOCplanner system-on-a-chip platform. The platform integrates a range of design technologies, design tools, and design methods that are invaluable to designers because they cover the range from system specification design to system evaluation. We intend to improve this platform in the future, in line with advance in semiconductor technology, to suit the needs of electronic product designers.

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