

Prospect of Si Semiconductor Devices in Nanometer Era

Shinichiro Kimura, Dr. Eng.
Digh Hisamoto, Dr. Eng.
Nobuyuki Sugii, Dr. Eng.

OVERVIEW: Silicon semiconductor (MOSFET: metal-oxide semiconductor field-effect transistor) dimensions are approaching the nanometer scale. The gate electrode size has already been reduced to 50 nm or less for the most advanced 90-nm technology nodes, and for the 65-nm nodes the size is expected to be 25 nm. A new guideline to replace the scaling rule is needed, and making use of the strain effect or 3D device structure design have attracted attention as a means of meeting that need. Technology that makes use of material strain requires highly accurate evaluation technology for strain and control of defects possibly caused by the strain. Substrate etching is a very important process in achieving a 3D MOSFET. Nanometer-scale precision, removal of processed surface damage and evaluation technology for that are essential.

INTRODUCTION

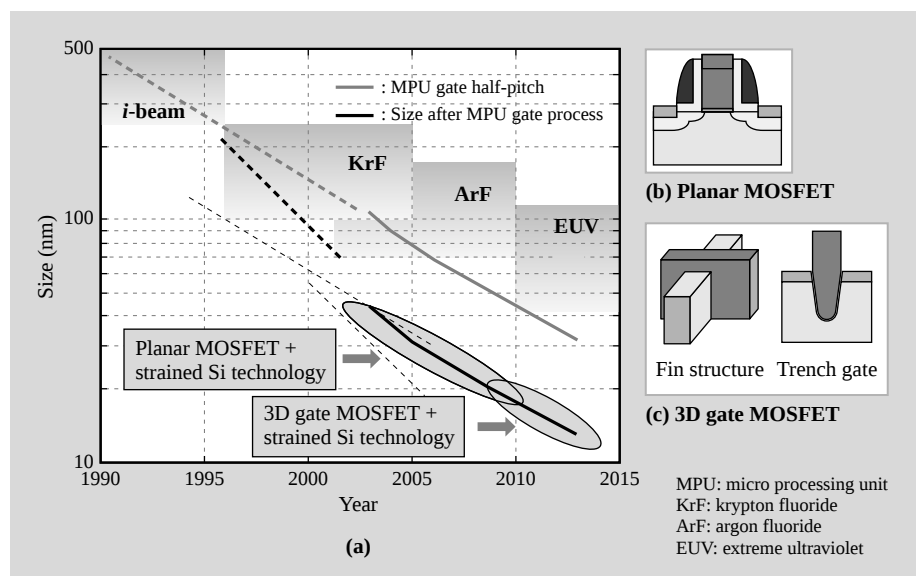
NUDGED by the promise of digital home appliances, the LSI industry got back onto the track of growth in the last half of 2003, and that situation is expected to continue in 2004 as well. WSTS (World Semiconductor Trade Statistics) estimates that the worldwide LSI sales for 2004 will be 19 billion dollars (about 20 trillion yen at 105 yen to a dollar)⁽¹⁾.

Process and device technology for fabricating LSI chips has entered the 90-nm node era, using 90-nm process technology defined in terms of the half pitch (the sum of the line width and distance between lines divided by two), as shown by ITRS (International

Technology Roadmap of Semiconductor)⁽²⁾. Recently, some high-performance microprocessors and large-capacity flash memory devices that employ 90-nm technology have begun to enter the market. The gate electrode dimensions of the MOSFETs (metal-oxide semiconductor field-effect transistors) used in those products are 50 nm or less. These dimensions are still large compared to what is considered the fundamental limit for device operation (≤ 10 nm), but, for various reasons, the reality is that it is becoming increasingly difficult to improve performance by using finer design patterns.

Against this background, experimentation that takes

Fig. 1—Change in Estimated MPU Gate Electrode Half-pitch Dimension and Size after Processing with Changes in Lithography Exposure Methods Shown by ITRS. MPU gate electrode size is becoming far smaller than half-pitch, and the rate of size reduction has been accelerating in recent years.



approaches to better device performance other than using the conventional scaling rule as the guideline for improvement has increased. In this paper, we consider these new approaches and outline recent process and device technology, such as using a strained substrate and a 3D structure while keeping fabrication technology and evaluation technology in mind.

NEW PERFORMANCE IMPROVEMENT GUIDELINE FOR MOSFETS

The ITRS points to a half pitch of 45 nm in 2010 and the MOSFET gate length of 18 nm is predicted for high-performance microprocessors. However, this goal is not easy to achieve with current planar MOSFET structures. Therefore ITRS proposes to depart from the approach that relies solely on finer design rules that have been taken up to now and adopt a new guideline. Typical experimental candidates for a new guideline include making use of the strain effect and a 3D fin structure for the MOSFET channel. In this section, we describe these two approaches from the device perspective.

Stress Control for Higher Si-MOSFET Performance

Strained Si technology, in which stress is applied to the channel region of the MOSFET, is attracting much attention as a promising means of improving performance even in the sub 90-nm region, where higher performance is difficult to achieve. When a Si crystal lattice is distorted by the application of stress, the symmetry of the isotropic Si crystal band structure is broken, and a split in energy levels occurs. The

change in band structure results in reduced carrier dispersion by lattice vibration and a reduction in effective mass, which improve mobility. Although the increase in mobility depends on the amount and direction of the strain, the electron mobility can increase by a maximum factor of two and the hole mobility can increase by a maximum factor of 1.5. The improvement in mobility is retained even for fine MOSFETs in which there is a saturation in carrier velocity. This rivals the performance gained by at least one generation of miniaturization.

Several methods of applying the stress have been proposed (see Fig. 2) ^{(3)–(5)}.

- (1) Application of external stress to an ordinary Si substrate (this method was proposed by Hitachi, Ltd. for the first time in 2000).
- (2) Epitaxial growth of a SiGe layer on the Si substrate followed by growth of a Si layer to create strain in the surface Si layer (bulk strained Si),
- (3) diffusion of Ge into the Si layer of an SOI substrate to form SiGe followed by growth of Si on that surface to create the strain (SGOI) and,
- (4) the transfer of bulk strained Si to another substrate that has an insulation layer, followed by removal of the SiGe to obtain a strained SOI that is free of SiGe (SSOI), and others.

SiGe is a mixed crystal composed of a solid solution of a certain amount of Ge in Si. The crystal lattice of Si increases in accord with the proportion of Ge in the mixture. If crystal (SiGe buffer layer) in which the crystal lattice is larger than the Si is covered with Si by epitaxial growth as shown in Fig. 3, Si atoms are forced to grow in alignment with the interatomic

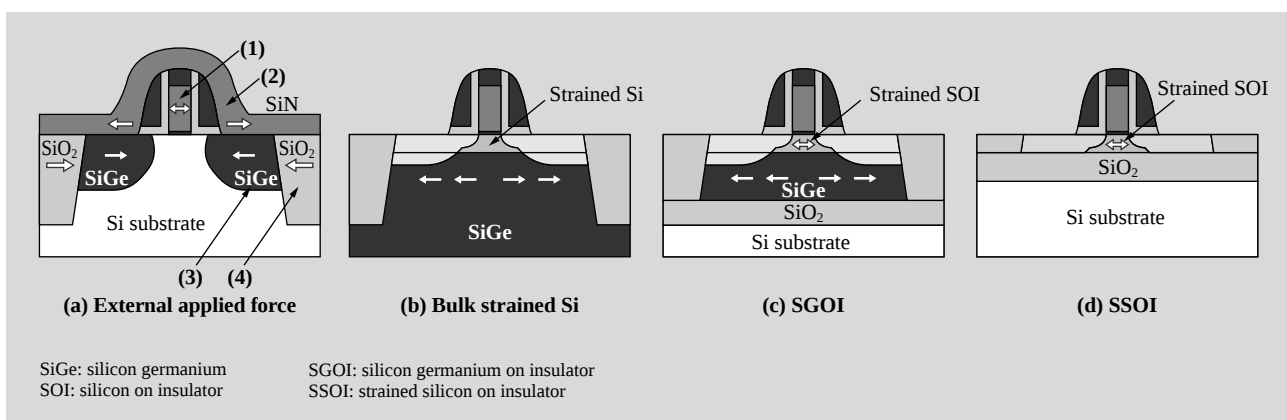


Fig. 2—Comparison of Channel Straining Methods.

In the application of external stress in (a), (1) employs stress from the gate electrode, (2) employs stress from the nitride layer (SiN), (3) employs stress from the SiGe embedded in the substrate, and (4) employs stress from the inter-device oxidation layer.

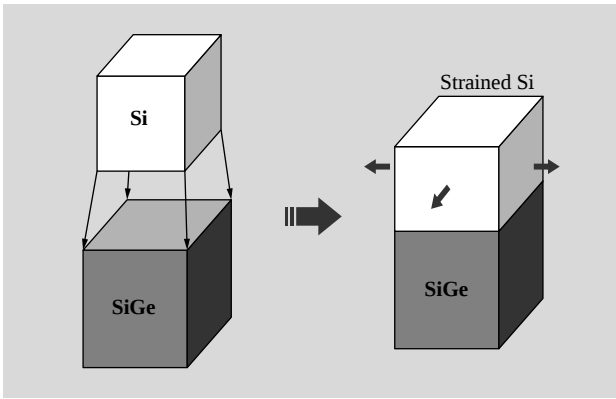


Fig. 3—Model of Introducing Strain by Epitaxial Growth of Si on SiGe.

It is possible to form a silicon layer with tensile strain by the epitaxial growth of silicon on an SiGe layer, which has larger lattice spacing than Si.

distance in the SiGe crystal. For example, if the Si is grown on SiGe that has Ge content of about 20%, the interatomic distance will be increased by about 0.8%, for which the calculated stress is about 1.4 GPa of tensile stress.

The strained Si-MOSFET involves a number of issues caused by the application of high stress to the channel region, the use of SiGe and other factors. We take up representative issues here:

(1) Crystal defects: the strained Si channel layer has the maximum permitted layer thickness (i.e. the critical layer thickness), and if that thickness is exceeded, dislocations will occur in the strained Si layer. These dislocations greatly increase the leakage current of the transistor. For the substrates of from 15 to 20% Ge that are being used in CMOS development, the maximum permitted strained Si layer thickness is only about 15 nm⁽⁶⁾, so care must be taken to avert reduction of the layer thickness in the transistor fabrication processes.

(2) Ge and oxidation and diffusion: if the thermal treatment during the transistor fabrication process is excessive, the Ge in the SiGe layer will diffuse into the strained Si. The diffused Ge will cause carrier scattering, sharply reducing the reliability of the oxide film and negatively affecting the transistor characteristics.

(3) Threshold voltage control: Si, strained Si and SiGe each have different bandgaps. This creates variation in channel surface potential, which results in variance in the threshold voltage. It is therefore necessary to devise a means of adjusting the threshold voltage to an appropriate value by controlling channel doping or the gate electrode work function.

(4) Low thermal conductance: the thermal conductivity of SiGe is an order of magnitude lower than that of Si and the same kind of self-heating phenomenon as is seen with SOI-MOSFETs has been observed (i.e. the channel temperature rises locally and reduces the output current of the transistor). While the effect on a digital circuit is small, this phenomenon may affect the performance of analog circuits.

Despite the significant number of issues in transistor fabrication described above, there is growing recognition that use of the strain effect is a necessary technology for MOSFETs in the sub 90-nm era. The reason for this, also given above, is that we cannot expect the same rates of improvement in individual transistor performance that we have seen in the past, even with further miniaturization. Technology for the introduction of strain is also applicable to the 3D MOSFET structures that we describe next. We believe that device technology in the 65- to 45-nm era and beyond will move in the direction of combining these two types of technology.

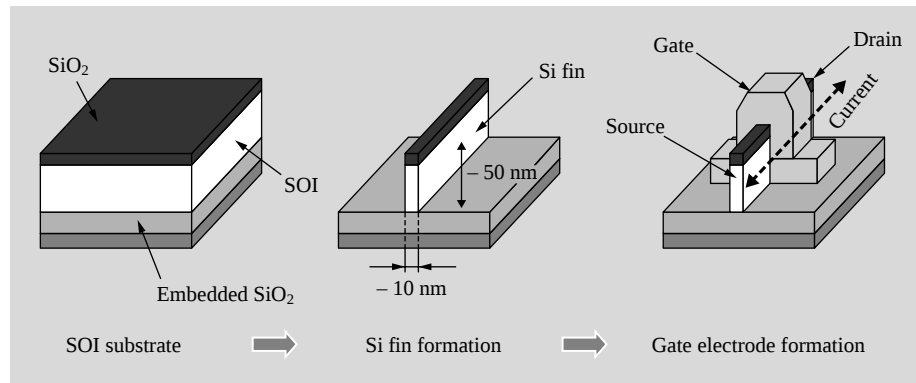
Fin Structure Devices

The MOSFET is an ideal form for semiconductor planar processing technology and device scaling has proceeded in step with advances in process technology. For example, reduction in gate electrode dimensions, which is the key to higher performance, is also a result of advancement in lithography technology. For the conventional planar structures, however, higher dopant concentration is required to control the short channel effect as scaling proceeds. The reason for this is that carrier mobility decreases, reducing device performance. Now that gate electrode size has reached 100 nm on the commercial level and 10 nm in the laboratory⁽⁷⁾, we are becoming fully aware of the limits of scaling.

As a way to extend the utility of scaling, changing from the planar structure that has been used up to now to a 3D channel structure is being considered. The 3D structure makes efficient use of the gate electric field effect to control the short channel effect. This makes it possible to keep the channel dopant concentration low and thus offers the potential of high device performance.

The fin structure Hitachi has developed is the most promising structure for a 3D MOSFET. This device has the same channel direction and wiring layout as does conventional MOSFETs, because the same planar etching technology is used. This structure was achieved for the first time in our Central Research Laboratory

Fig. 4—Fabrication Process for Fin Structure MOSFET. The Si layer on an SOI substrate is etched to a thin wall shape (fin). A gate oxidation layer is then formed across the fin, resulting in a gate electrode that straddles the fin.



using selective oxidation⁽⁸⁾. We subsequently reported a fin-FET (field-effect transistor) that employed an SOI wafer. In recent years, devices that employ the fin structure have been announced by various companies⁽⁹⁾.

A typical forming process is shown in Fig. 4. The fin is formed by etching Si single crystal and then forming the gate electrode across the fin. In this way, a 3D channel structure can be formed by using planar process technology. The size of the fin depends on the generation of the device, but a 15-nm width and a 50-nm height are typical. For the gate electrode, however, the process must be highly selective because the gate is formed across the high step formed by the fin.

Two advantages offered by the device are that the substrate wall serves as a channel, and that the gate electrode covers both sides of the fin, thus forming a double gate structure. If the channel wall serves as the channel, the channel width is determined by the height of the fin. It is therefore substantially larger than the layout width and the current drivability is increased. In addition, the double gate structure increases the control of channel potential by the gate electrode, thus making it possible to suppress the short channel effect without a high channel dopant concentration. As a result, a high carrier mobility and carrier density can be obtained and a reduction in gate parasitic capacitance can also be expected.

Fin structure devices, on the other hand, share the problems caused by an ultra-thin SOI layer. Those problems include:

- (1) the threshold voltage cannot be controlled by dopant concentration,
- (2) variance in the SOI layer thickness invites variance in the threshold voltage,
- (3) channels are formed on fin sidewalls damaged by etching,
- (4) increased parasitic resistance and parasitic capacitance due to the thin fin structure, and

(5) the difficulty of forming ESD (electrostatic discharge) devices and I/O (input-output) devices.

The fin etching technique plays an important role in the solution of these problems.

MEMORY DEVICE TECHNOLOGY

This section concerns memory devices, LSI chips that store data. The DRAM (dynamic random access memory) that serves as the main memory for PCs and servers and the flash memory that is used to record images in digital cameras and store data in mobile phones are typical examples of high-capacity memory chips. The latter devices feature non-volatile data storage and have an expanding range of applications. In terms of memory capacity, too, flash memory devices are moving ahead of DRAM. Here, however, we discuss DRAM from the perspective of 3D device structure.

DRAM uses a single switching transistor (MOSFETs are used) and a single charging capacitor to represent one bit. The smallest unit of a memory device is called a memory cell. It is basically a simple structure, and this is the most important factor in making high-density DRAM chips. Nevertheless, although the latest 512-Mbit and 1-Gbit DRAMs use the conventional basic structure unchanged, the miniaturization of that structure requires very advanced micro-fabrication technology. In particular, 3D structures are used to the utmost to maintain the surface area of the capacitors that store information as electrical charges in the limited memory cell area, because the amount of charge held by the capacitor is more or less determined by its surface area. We will explain this using a stacked capacitor cell, in which the capacitor is placed on top of the MOSFET as an example (see Fig. 5).

The capacitor structure consists of a dielectric layer sandwiched between the lower electrode and the upper electrode, with the lower electrode making electrical

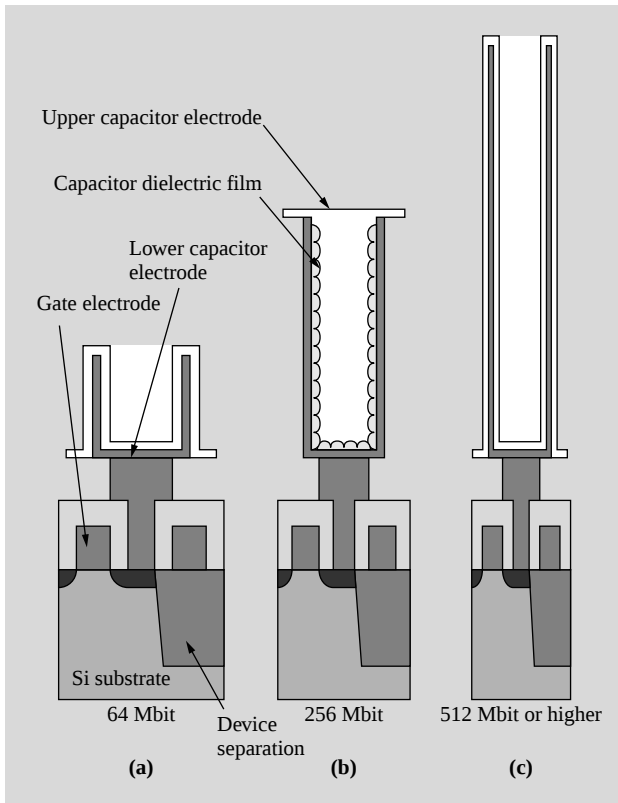


Fig. 5—Changes in Memory Cell Structure.
Transition has been from cylinder structure to deep trench + uneven surface and then to cylinder structure again.

contact with one of the diffusion layers of the MOSFET. Typical examples of the latest capacitor structures are shown in Fig. 5⁽¹⁰⁾. For 64-Mbit chips, the capacitor structure is the so-called cylinder type, which allows use of both the inner and outer walls of the lower electrode. This design keeps down the height of the electrode. For the 256-Mbit device, on the other hand, generally a deep trench is formed in a thick dielectric layer deposited on the upper layer of the MOSFET, making use of the inner wall of the lower electrode. To further increase the capacitance of this structure, forming of minute silicon HSG (hemispherical grains) on the electrode or other such techniques can be used⁽¹¹⁾.

For the 512-Mbit and 1-Gbit chips, however, the cell surface area must be reduced even further, so this deep trench structure must be even deeper. The small hole diameter makes it impossible to form the HSG on the inner wall of the lower electrode to increase capacitance. Therefore, the cylinder type capacitor has been resurrected for DRAM that targets the recently reported sub 90-nm nodes. The dimensions are 150 nm or less for the inner diameter of the cylinder, 50 nm or less for the thickness of the cylinder wall,

and 1.4 μm for the cylinder height. The aspect ratio is 10 : 1, truly a nanostructure chimney⁽¹²⁾. In addition, the distance between adjacent capacitors is 100 nm, so to prevent them from touching each other, the lower electrode of each cylinder must be firmly self-supporting. The process of forming the cylinder-type capacitor requires processes for forming the holes in the oxidation layer, removal of the oxidation layer and cleaning. In particular, the oxide layer removal and cleaning are wet etching processes in which the slight gaps between cylinder capacitors are filled with etching solution. The surface tension of the etching solution may pull adjacent capacitors together and break them. For this reason, the capacitor must be firmly self-supporting.

Major changes are also imminent for switching MOSFETs. For sub 90-nm DRAM, the gate electrode size of this MOSFET is reduced to 80 nm. In reducing the MOSFET gate electrode size, the substrate dopant concentration must be increased according to the scaling rule as described above. However, higher dopant concentration degrades the information retention capability of the DRAM. This degradation is caused by the leak current that flows between PN (positive-negative) junctions as the electric fields of the PN junctions increase. Up to now, the data retention characteristics have been improved as miniaturization proceeded by optimization of ion implantation conditions and annealing for control of the dopant distribution.

However, for the ultra-small gate electrode size of 80 nm, it is expected to be difficult to cope with this problem by the control of dopant distribution alone. What has been proposed instead, is the trench

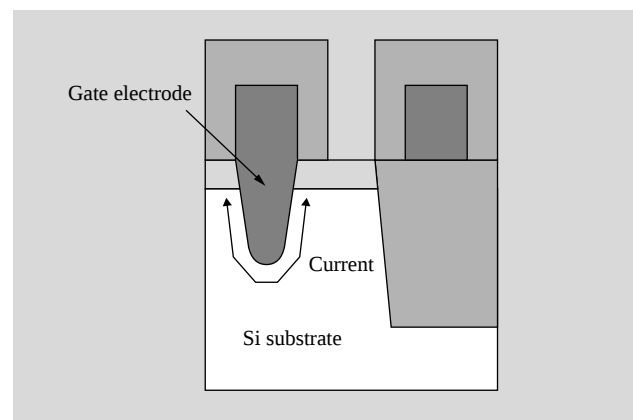


Fig. 6—Trench Gate MOSFET.
The current flow follows the shape of the groove formed in the substrate, so the effective current path can be lengthened, improving the short-channel characteristic.

MOSFET, which makes use of the side walls of a trench as shown schematically in Fig. 6⁽¹³⁾. Two effects can be expected from using the trench MOSFET. One is that, although the planar gate electrode size of the MOSFET gets smaller, the path of the current flow can be made longer. The other effect is suppression of the increase in electric field strength in the vicinity of the PN junctions that was described above. The latter effect results from the separation of the bottom of the channel and the diffusion layer.

For the trench MOSFET, the threshold voltage is greatly dependent on the shape of the trench⁽¹⁴⁾. There is also much concern regarding reliability because it is necessary to form the gate oxidation layer on a substrate surface that has been damaged by etching. We believe, however, that it remains an effective candidate for satisfying the special requirements for a DRAM switching MOSFET.

EXPECTATIONS REGARDING FABRICATION AND EVALUATION TECHNOLOGY

Changes in the device structure and the substrate necessitate changes expectations in the process technology and evaluation technology as well (see Table 1). For the strained Si method, which makes use of layer stress, technology for freely changing the stress of layers is needed. When strained Si substrate is used, layer thickness is only about 15 nm, so prevention of layer thinning during the process steps is required. Existing etching processes require various wet etching and sacrificial oxidation processes prior to the gate oxidation layer. Those processes cause a substrate removal of about 10 nm. For strained Si substrates and ultra-thin SOI substrates, however, such substrate removal cannot be allowed. For evaluation technology, a means for local measurement of stress is needed. At present, lattice strain is measured by cross-sectional TEM (transmission electron microscope) and the stress is obtained from these measurements, but from the viewpoint of wafer processes, a nondestructive evaluation is desired. In addition, threading dislocations (a type of dislocation that originates in the SiGe layer and pierces the strained Si region to terminate at the surface), which are a problem for strained Si substrates, have a low density of $<10^5/\text{cm}^2$, and no accurate method of evaluating their presence has been established. The evaluation of dislocations is important for increasing substrate quality.

For the fin structure and trench gate structures, on the other hand, channel regions must be formed on Si surfaces that have been subjected to dry etching and

TABLE 1. Requirements for Fabrication and Evaluation Technology

The technology required for fabrication and evaluation of the strained Si, fin structures and grooved gate structures that conform to the new scaling guidelines are summarized here.

	Fabrication technology	Evaluation technology
Strained Si	• Control of substrate removal • Control of layer stress	• Measurement of threading dislocation density • Measurement of local stress
Fin structure trench gate	• Extremely low-damage Si etching • Selective etching	• Measurement of 3D structures • Quantification of damage

other such processes. Dry etching results in C, O, H and other such etching gases penetrating the substrate and damage to the surface of the electrode. Up to now, regions of about 10 nm have been removed by sacrificial oxidation or other such methods. For nanometer regions, however, etching technology that does not cause damage is needed. Furthermore, technology for highly accurate measurement of 3D shapes is essential. The variance in device characteristics has increased with miniaturization. The variance depends on shape, so accurate evaluation of shape is basic to reduction in the variance.

CONCLUSIONS

More than 30 years have passed since the Intel Corporation developed the 1-kbit DRAM in 1970. Between that time and now, fine process technology has advanced continuously and the scale of integration has increased by a factor of one million. However, the area of a chip is no larger than a thumbnail. MOSFET devices have crossed the submicron and 0.1- μm barriers, and we have pushed forward on the path of miniaturization. The result is a gate length of 50 nm. We believe that LSI miniaturization and functional advancement will continue in the future, and that by expanding the scope of application, we believe these chips will continue to have an increasingly intimate presence in our lives.

On the other hand, it is an unmistakable fact that clouds are appearing on the path of miniaturization that has been followed up to now. Although the ITRS predicts an 18-nm size for the year 2010, this length is a mere 100 silicon atoms lined up. Some approach other than miniaturization is needed, and a new direction that focuses on device structure will improve

performance with the 3D structures and new Si substrate described in this paper. In addition to that, device fabrication technology and module technology are also receiving attention, and higher integration scale by multi-stage layering for memory chips, and greater functionality by stacking different types of chips and other such techniques are becoming common technology for mobile phones and other such devices. With the integration of these kinds of technology, LSI performance will continue to improve in the future as well.

REFERENCES

- (1) WSTS 2003.
- (2) ITRS 2003.
- (3) F. Ootsuka et al., Technical Digest, Int. Electron Devices Meeting, p. 575 (2000).
- (4) K. Rim et al., Technical Digest, *ibid.*, p. 49 (2003).
- (5) T. Ghani et al., Technical Digest, *ibid.*, p. 978 (2003).
- (6) J. W. Matthews et al., *J. Cryst. Growth* 27, p. 118 (1974).
- (7) H. Wakabayashi et al., Technical Digest, Int. Electron Devices Meeting, p. 989 (2003).
- (8) D. Hisamoto et al., *ibid.*, p. 833 (1989).
- (9) J. Kedzierski et al., *ibid.*, p. 247 (2002).
- (10) T. Adachi, *Nikkei Microdevices*, Nov. p. 83 (2003) in Japanese.
- (11) H. Watanabe et al., Ext. Abstract of 22nd Conf. Solid State Devices and Materials, p. 869 (1990).
- (12) W. K. Park, et al., Technical Digest, Int. Electron Devices Meeting, p. 819 (2002).
- (13) J. Kim et al., Dig. Tech. Papers, Symposium on VLSI Technology, p. 11 (2003).
- (14) J. Tanaka et al., *IEEE Electron Device Letters*, 14, p. 396 (1993).

ABOUT THE AUTHORS



Shinichiro Kimura

Joined Hitachi, Ltd. in 1980, and now works at the ULSI Research Department, the Central Research Laboratory. He is currently engaged in the development of non-volatile memory devices.

Dr. Kimura is a member of The Institute of Electrical and Electronics Engineers, Inc. (IEEE) Electron Device Society and The Japan Society of Applied Physics (JSAP), and can be reached by e-mail at sayo@crl.hitachi.co.jp.



Digh Hisamoto

Joined Hitachi, Ltd. in 1986, and now works at the ULSI Research Department, the Central Research Laboratory. He is currently engaged in the development of embedded memory devices.

Dr. Hisamoto is a member of IEEE Electron Device Society, The Institute of Electronics, Information and Communication Engineers (IEICE) and JSAP, and can be reached by e-mail at hisamoto@crl.hitachi.co.jp.



Nobuyuki Sugii

Joined Hitachi, Ltd. in 1988, and now works at the ULSI Research Department, the Central Research Laboratory. He is currently engaged in the development of SiGe heterostructure devices and strained silicon devices.

Dr. Sugii is a member of JSAP, and can be reached by e-mail at sugii@crl.hitachi.co.jp.