Inspection-analysis Solution for High-quality and High-efficiency Device Manufacturing

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OVERVIEW: The mass-production of a 90-nm node device and the development of a 65-nm node device were started in earnest in 2004. The manufacturing technology will be needed during the development of advanced devices to control and optimize the process condition and parameters by using the electrical characteristics during the development of advanced devices. Hitachi Group proposes inspection and analysis solution, ones that focus on in-line electrical characteristics monitoring. This solution consists of advanced inspection and analysis tools and application technology.

INTRODUCTION

THE mass-production of 90-nm node devices and the development of 65-nm node devices were started during 2004. In order to start mass production as soon as possible, we need to optimize the process parameters in the early stages of manufacturing. A reliability enhancement, yield improvement, and quality control will be important for mass-production. The following technologies are required in this process, including the development of new production and QTAT (quick turnaround time) optimization of manufacturing and yield enhancement.

(1) In-line metrology of every CD (critical dimension) based on layout information,
(2) in-line defect/particle level monitoring and a feedback system,
(3) monitoring and quality control of device electrical characteristics, and
(4) defect root cause analysis and efficient information delivery for feedback to the manufacturing condition.

To meet these needs, we have to establish a total inspection and analysis solution, focused specifically on electrical failures, such as contact failures and leakage defects, which directly affect the device electrical characteristics (see Fig. 1).

REQUIREMENTS FROM DEVICES

Fig. 2 shows the device structure of a 65-nm node

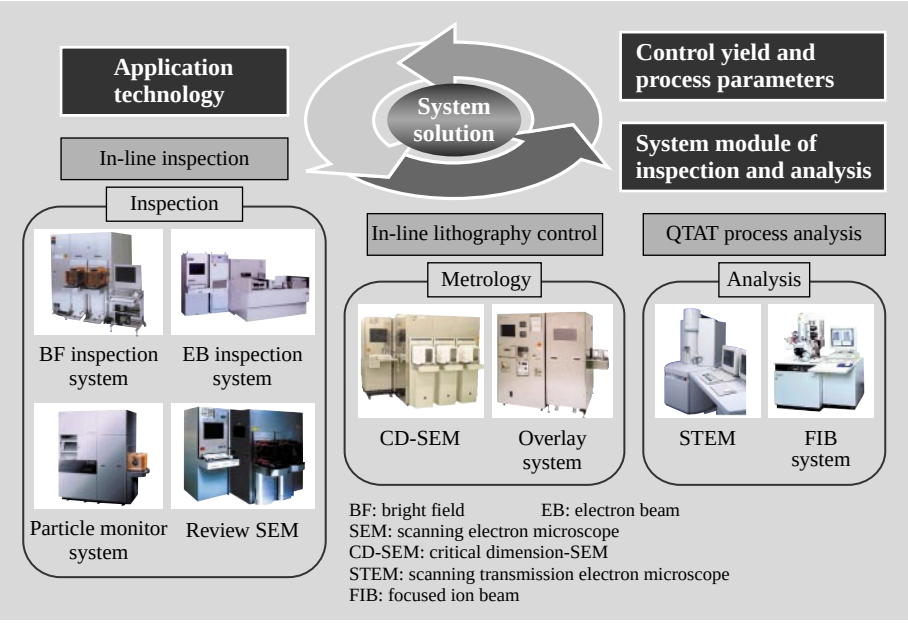


Fig. 1—Metrology, Inspection, and Analysis System Developed by Hitachi Group for Semiconductor Devices.
Hitachi Group has developed metrology, inspection, and analysis tools in addition to an inspection and analysis solution for high-quality and highly efficienct semiconductor production.

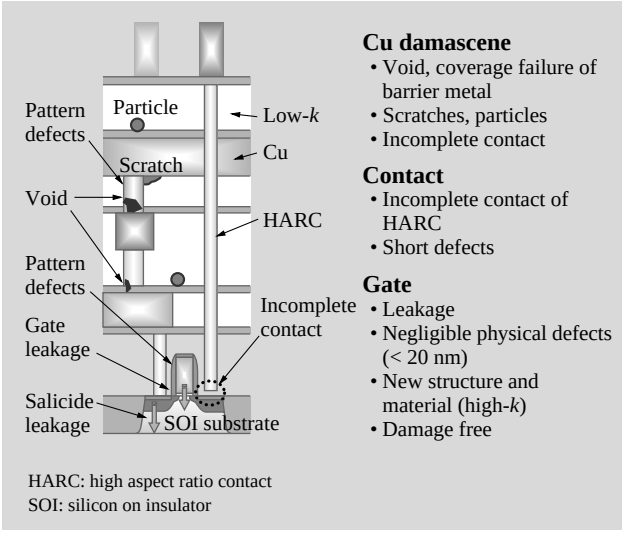


Fig. 2—Structure of Semiconductor Device and Defect Type at 65-nm Node.
Use of new material such as low-k, high-k is begun. Performance requirements (high speed, low power) are increased.

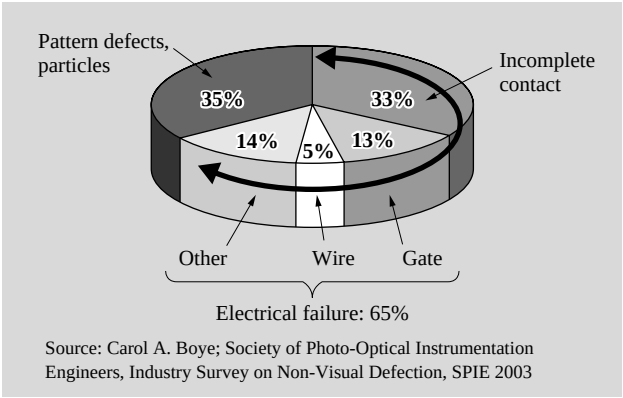


Fig. 3—Ratio of Electrical Failure within Defects.
Analysis of cause of low yield by SEMATECH Inc. showed ratio of electrical failure have been more than 65% .

and the required items for an in-line inspection.

A multi-structure gate in the front end of 65-nm nodes and beyond was developed for high-speed and high-performance devices. Strained silicon and SOI were applied as part of a new process technique to control punch through, to reduce leakage current, and to allow for low power. Also, a high-*k* material was applied as gate dielectrics for the reliability of gate characteristics. In the back end of the devices, multi-layered Cu wiring of a dual damascene structure was introduced, and low-*k* material was applied as wiring dielectrics. Because of the multi-layered wiring process and damascene structure, the number of via holes was increased, and the yield impact by the via hole process was increased(1).

Based on these trends, the required items to inspect DOI (defect of interest) are:
(1) detection of voids of the Cu wiring process including via holes,
(2) high aspect ratio contact hole inspection and short detection,
(3) detection of leakage of gate dielectric and salicide fine pattern defects such as a stringer or pit, and
(4) detection of various defects caused by a new material and a new structure such as a high-*k* or low-*k* multi-gate structure.

A highly accurate measurement of every CD and structure evolving along with process shrinkage is required, and on top of this, measurement/inspection of electrical characteristics and process results of a whole wafer are also required. Fig. 3 shows an example of classification of probe testing failures. The electrical failures caused by contact and wiring process failures was more than 60%. This result shows that the contact failures and wiring process inspection are very important to yield enhancement(2).

SOLUTION FOR ELECTRICAL FAILURE

Based on previous requirements, Hitachi High-Technologies provides electrical failure detection techniques with an EB inspection tool, an efficient and quick classification technique by a review SEM, and a QTAT analysis technique to analyze the defect root cause using analytical tools.

Electrical Failure Detection

The EB inspection tool is effective to detect a hidden electrical failure such as an incomplete contact, short wiring defect, and voids. The principle of EB inspection is as follows; a large current EB is irradiated to a semiconductor wafer surface, and secondary electrons are detected. The number of secondary electrons, which are emitted to the detector, is affected by surface charging voltage. Using this phenomena, the electrical condition inside the device can be detected by the contrast in the SEM image (detection of voltage contrast)(3). Fig. 4 shows these principles. For example, when the EB is irradiated at an incomplete contact, the charging voltage of this incomplete contact increases over that with the normally opened contact hole. Because of this charging condition difference, the number of secondary electrons, which are emitted from the bottom of the hole, is different between the normally opened hole and the incomplete hole. For a positive charging condition, the normally opened hole is observed as bright contrast, and the incomplete hole is observed

as dark contrast. Not only contact failures but also short defects, leakage, broken wire, resistance failures, and capacitance failures can be detected using these voltage contrast phenomena.

Fig. 5 shows an example of applying EB inspection to via holes inspection at the peripheral pattern of advanced DRAM (dynamic random access memory) production. Incomplete contact failures at the layer of aspect ratio 10 were detected from this example. These results show that EB inspection is effective as a contact process monitoring tool[4].

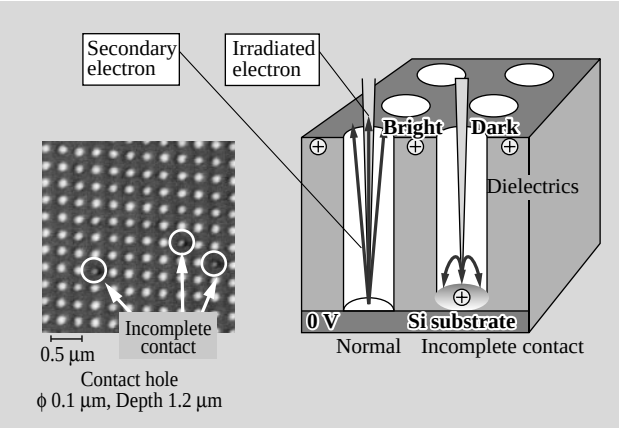


Fig. 4—Voltage Contrast Principle and SEM Image of Incomplete Contact.
With positive voltage contrast mode, contrast of normally opened contact hole is bright and contrast of incomplete contact hole is dark. It is because the number of secondary electrons reaching detector is changed by the charging condition at the bottom of hole.

Defect Classification

Review SEM is an effective tool to observe the defects which are detected by other tools with high-resolution images and to classify the types of them. Because various kinds of defects occur during the development stage of new production, we need to extract the serious defects efficiently and to review them quickly. As shown in Fig. 6, the review SEM must review and classify the particles, pattern defects, and electrical failures, and identify the killer defects from the defects that are detected by the various inspection tools such as EB inspection, BF inspection, and a particle monitor.

Fig. 7 shows the review SEM images of the defects

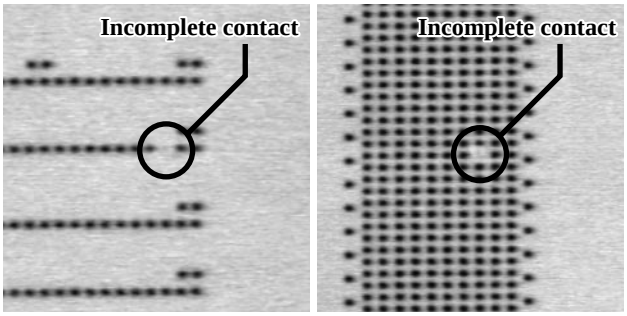


Fig. 5—Example of Application of EB Inspection to Contact Layer at Peripheral Pattern of DRAM Products.
Incomplete contact failures of the holes of aspect ratio 10 are detected stably.

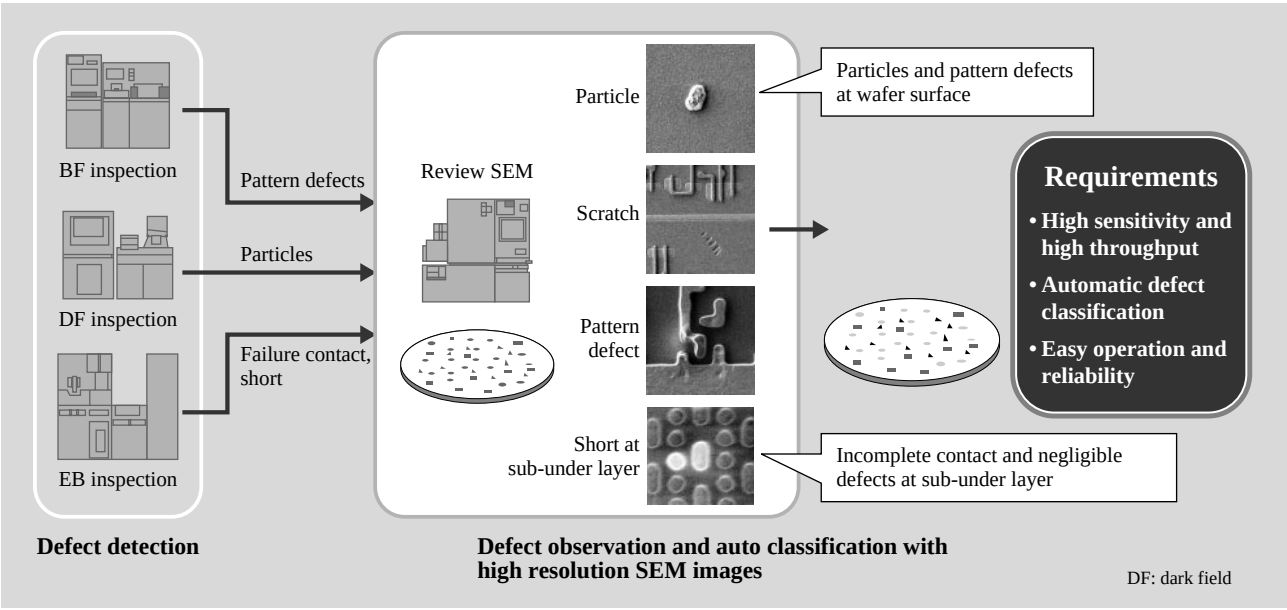


Fig. 6—In-line Defect Classification Station; Review SEM.
Review SEM classifies particles, pattern defects and electrical failure, and extracts killer defects from the larger number of the defects detected by various inspection tools.

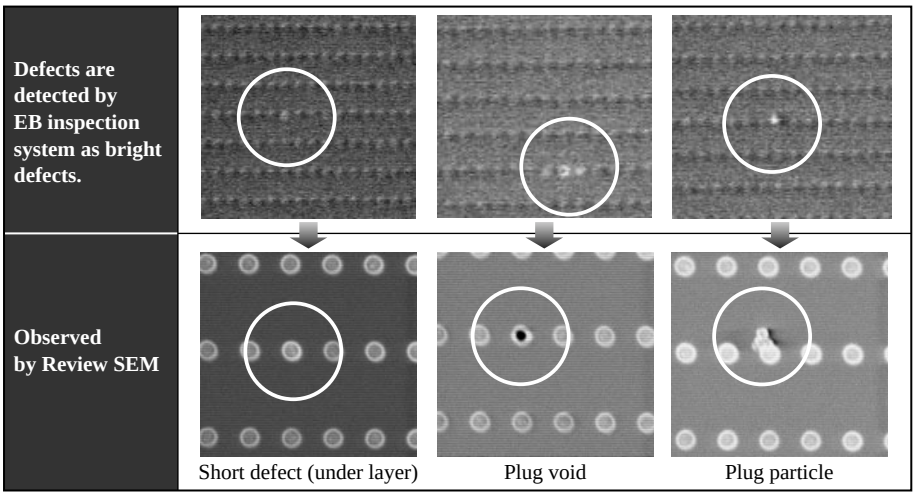


Fig. 7—Review SEM Image of Detected Defects Using EB Inspection as Brighter Defect Compared with Normal Bit. Detailed information of defects is obtained by high resolution SEM images.

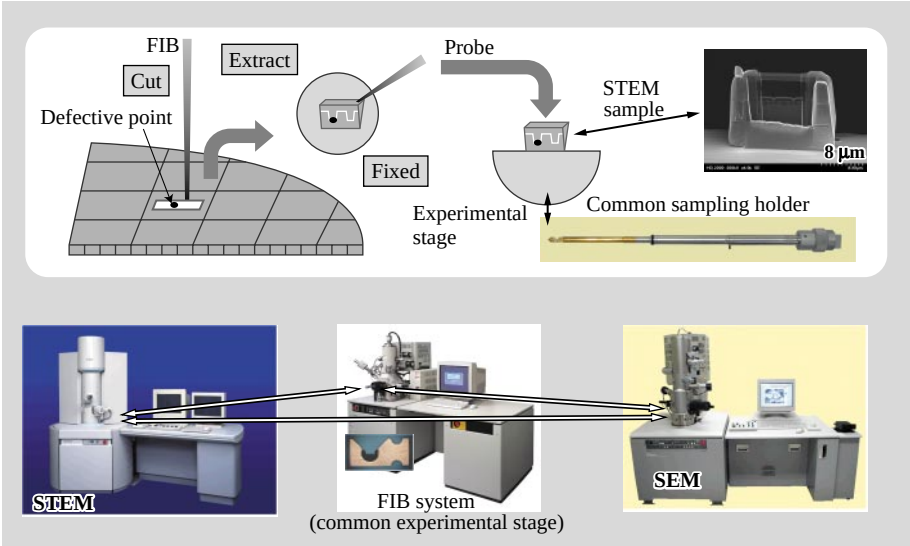


Fig. 8—Hitachi Group's Failure Analysis System. Defect point is sampled by micro-sampling technique of Hitachi FIB and observed by STEM and high resolution SEM.

detected with the EB inspection tool at a brighter contrast than the normal bit. The first type of defect is a short defect of the under layer. The second type is a small particle in a plug pattern. The third is a void of the plug. These images indicate that a high-resolution image is necessary to classify the type of defect accurately.

At the image creation of EB inspection, a large current EB such as 100 (nA) is used and the high SN (signal to noise) ratio image is created by just a single scan, not by superimposing. On the other hand, the beam current of a review SEM is of a pA order to achieve the high-resolution. The review SEM may be unable to recognize some electrical failures, which are detected with the EB inspection tool. This is caused by the voltage contrast sensitivity being affected by an irradiated beam current. To solve this problem, a voltage contrast control function was introduced into a Hitachi review SEM. It enhanced the sensitivity of the voltage contrast observation.

Failure Analysis

The defect root cause analysis of hidden electrical failures requires a cross-sectional observation by high-resolution SEM and STEM. During the failure analysis, a Hitachi micro-sampling method (see Fig. 8) was useful to cut the defective part of the sample out of the wafer. Several ways are used depending on the defect type[6), (7)].

INSPECTION AND ANALYSIS APPLICATION

The data acquired by applying the aforementioned inspection, review, and analysis techniques is shown in this chapter.

The first set of application data is the electrical failure detection at the SAC (self-aligned contact) layer (after it is plugged by poly-silicon) of DRAM production using Hitachi EB inspection tool. The DOI

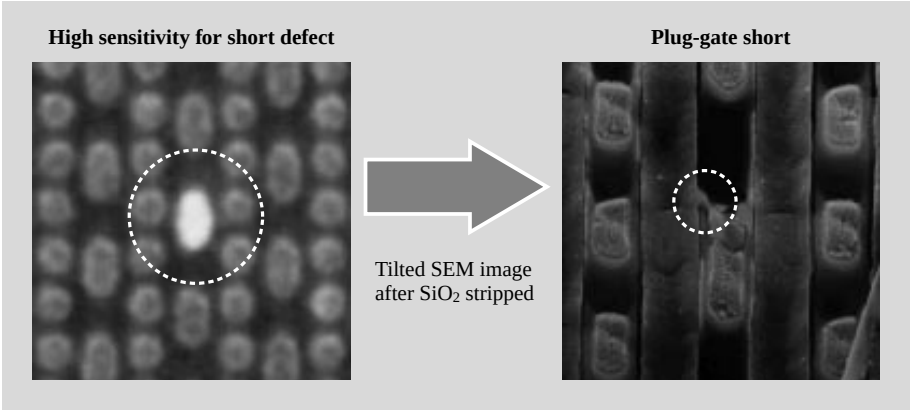


Fig. 9—Application Example of Review SEM Observation of Defect Detected by EB Inspection.
Short defects between plug and gate have been observed after stripping surface oxide film.

A. Miura et al. ISSM 2002

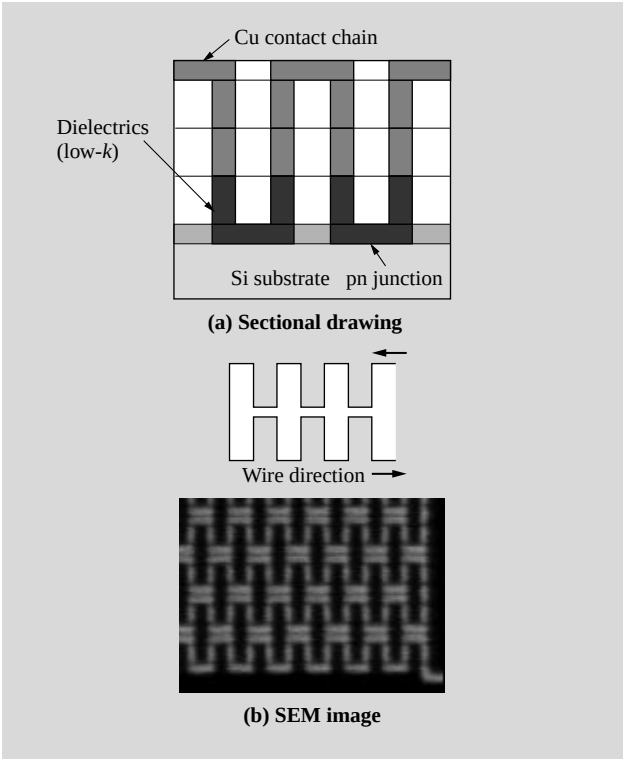
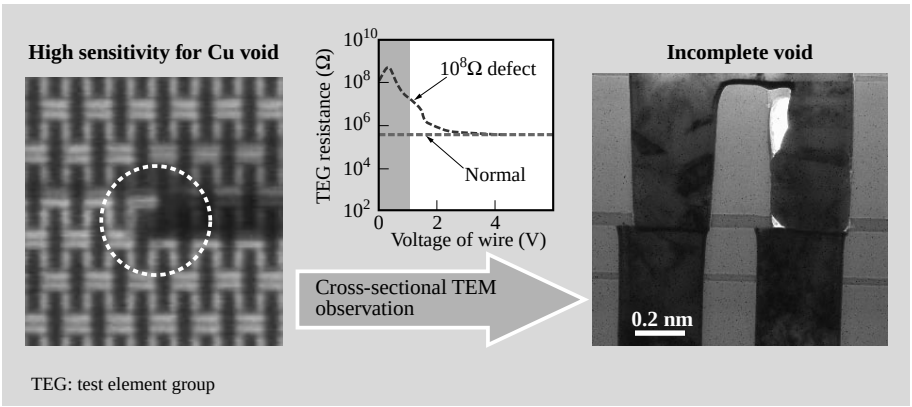


Fig. 10—Structure of Cu Contact Chain Test Pattern.
Test pattern structure is arranged using highly dense contact chain.

of this layer was short defects. The brighter plugs compared with the normal bit were detected by this in-line EB inspection. These defects were classified as electrical failures by Hitachi review SEM. The top oxide layer was stripped off based on this information, and defects were found to be plug-gate short (see Fig. 9)[8].

The second application is the Cu wiring test pattern inspection. The DOI of this inspection is the Cu void. Fig. 10 shows the test pattern structure. The contact chain pattern was inspected. The point of contrast change was detected inside the contact chain pattern using Hitachi's EB inspection tool. The *I-V* characteristics between both ends of the wiring of the wiring defect point were evaluated. Fig. 11 shows the result of the *I-V* characteristics. At the high contrast point, the resistance of Cu wire was higher compared with the normal point. However, the resistance of some of the defects point was reduced rapidly, and the voltage contrast became the same as normal wire, when the voltage applied to the both ends of the defect point was raised above 2–3 V. This result indicates that we need to control charge voltage to detect the high resistance defects with high sensitivity. These defects



TEG: test element group

Fig. 11—Analytical Result of Defects inside Contact Chain.
Result is shown of electrical characteristics analysis and cross-sectional observation for Cu void.

were analyzed by a cross sectional STEM observation using micro sampling by our FIB inspection system. These defects were the coverage failures of the barrier metal (see Fig. 11).

This data shows that the in-line inspection is effective to detect defects affecting transistor characteristics at the front end and wiring process yield at the back end. Also, the QTAT defect root cause analysis is effective to optimize the process parameters, and as a result, enhances yield.

CONCLUSIONS

The integrated process from inspection/measurement to analysis becomes more important to reduce the development cycle period because the production cycle has been shortened and custom small amount production such as SoC (silicon on chip) has been introduced. These trends indicate that the full process of inspection and an analysis solution is required to yield rapid enhancement and QTAT process optimization.

In addition, the need for an inspection and analysis technique increased because of the variety of processes, materials, and products. An effective and smart solution for each product and fab is now required. Controlling damage caused by EB or laser beams, used in the inspection and metrology tools for new materials, is also important in manufacturing. We will develop a solution that includes this kind of interaction between a charged particle beam and materials.

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