

# Electronics

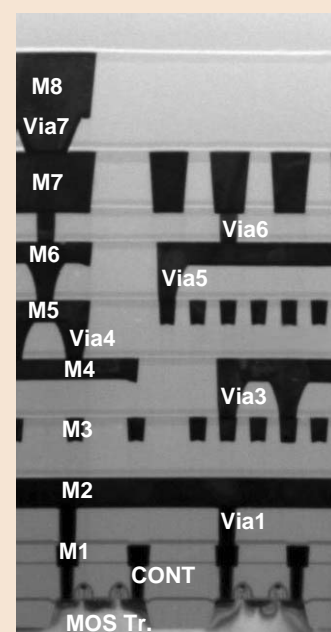
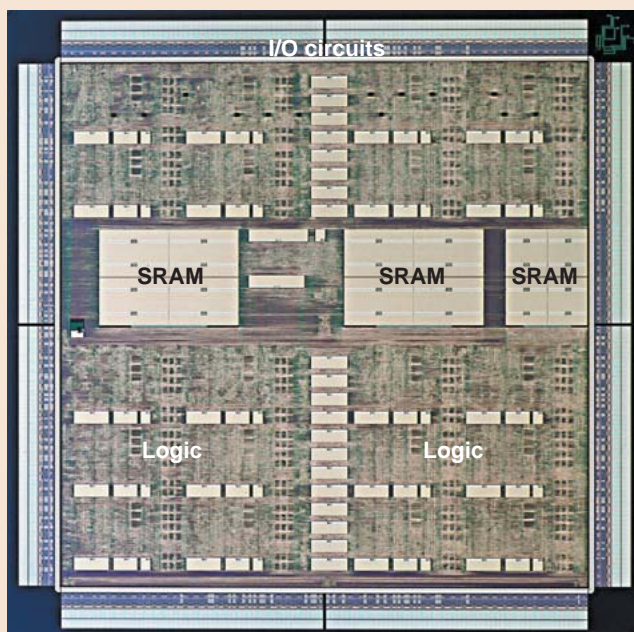
## 110-nm CMOS ASIC HDL4P Series with High-speed I/O Interfaces

Hitachi has released the high-performance 110-nm CMOS ASIC HDL4P series with high-speed I/O interfaces. Up to 1 GHz of operation frequency is possible because the series uses 80-nm-gate-length MOS transistors, which operate at 1.2 V. A fine 360-nm pitch and 9-metal-layer wiring makes possible a highly integrated SOC (system on chip) with up to 34 M useable gates. The small resistance of copper wiring and the small parasitic-capacitance of low-*k* dielectric layers reduce wire delays. There are three types of high-speed, standard and low-leakage gates in the standard cell library for the same function. Since high-speed gate uses the low-threshold MOS transistors, the leakage current is large. On the other hand, the low-leakage gate with the high-threshold MOS transistors operates at low frequency. The standard type is in the middle between the high-speed and the low-leakage ones. Sophisticated mix-use of three gate types enables high frequency operation with relatively small leakage currents. Multi-port SRAM macros allow up to 1-GHz operation. Multi-port SerDes (serializer and de-serializer) and CML (current mode logic) I/O circuits can operate at up to 5 GHz for high data transmission rates between LSIs. Both clock synchronous and asynchronous type SerDes can communicate with and without 8B/10B coding. Various kinds of high-speed I/O circuits can be used for connecting by proper signal voltage levels with other LSIs. Several kinds of IP (intellectual property) cores for communication, such as PCI Express and 10 G Ethernet, can be used. High pin count and low thermal resistance package line-up can also be used. The maximum pin count of an FC-BGA (flip-chip ball grid array) package is

2,116 using the C4 (controlled collapse chip connection) technique. The maximum total power consumption is 60 W. The use of Hitachi's in-house DFT (design-for-test) tool, Singen, and fault diagnosis tool, Kogoro, guarantees high-speed and high-quality LSIs. Singen generates test circuits for both logic and memory BISTs (built-in self-tests). Any multi-phase and local clocks can be used with the tool. Test patterns are generated inside the chip and LSI tests are executed at the same frequency as the chips are used at. The HDL4P series is suitable for high-speed applications such as supercomputers, servers, and storage and network equipment.

[Main features]

- (1) Process technology: 110-nm CMOS
- (2) Gate length of MOS transistors: 80 nm
- (3) Internal power supply voltage: 1.2 V
- (4) Power supply voltage for I/O circuits: 3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
- (5) Number of useable gates: 34 M
- (6) Number of metal layers: 6 for fine pitch, 2 for coarse pitch, 1 for power
- (7) Maximum system frequency: 1 GHz
- (8) Power consumption: 16 nW/MHz/gate (with 100% operation rate)
- (9) Memory: 1-4 ports, up to 2.3 Mbit
- (10) Package: high-performance BGA package (up to 784 pins) and flip chip BGA (up to 2,116 pins)



Microphotograph of HDL4P example chip (left) and TEM (transmission electron microscope) image of cross section of MOS transistors and metal layers (right)

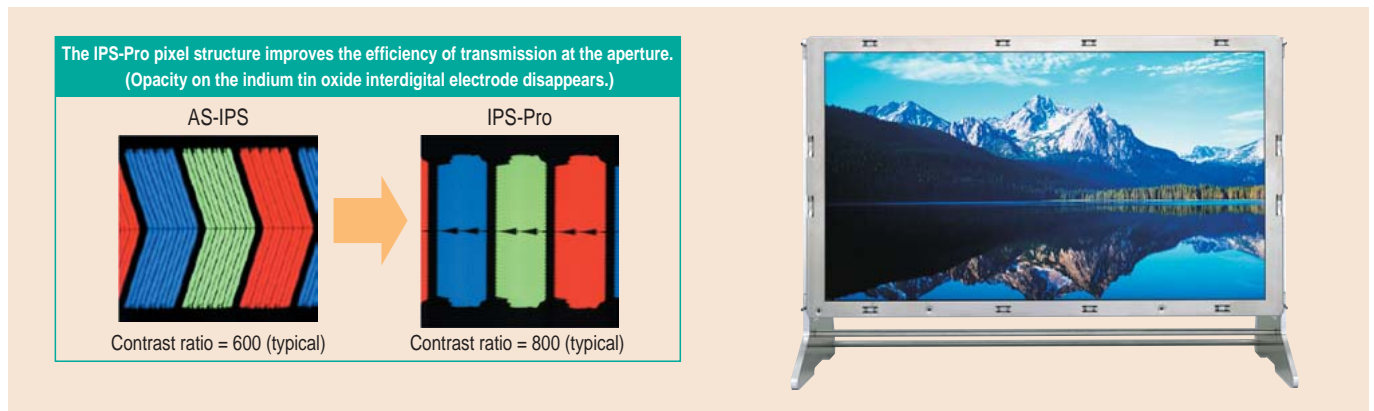
## 80-cm (32-in, 16:9) TFT LCD Module for TV

Consumers of LCD TVs demand a screen aspect ratio of 16:9, which is suited to high-definition broadcasts. To meet this demand, Hitachi has developed a 80-cm (32-in, 16:9) TFT (thin film transistor) LCD module for TV.

In addition to the super-wide viewing angle and smooth motion picture suited to LCD TVs, this product has a front contrast of 800:1 using IPS-Pro (in-plane switching *provectus*) technology, which has top-class contrast performance.

### [Main specifications]

- (1) Number of pixels: 1,366 (horizontal) × 768 (vertical)
  - (2) Brightness: 500 cd/m<sup>2</sup>
  - (3) Contrast ratio: 800:1 (front)
  - (4) Color reproducibility: 72% (ratio to NTSC standard)
  - (5) External dimensions (mm): 780 (wide) × 450 (high) × 50.5 (thick)
- (Hitachi Displays, Ltd.)



Comparison between IPS-Pro technology with high-contrast and AS-IPS (advanced super in-plane switching) technology (left) and external view of 80-cm (32-in, 16:9) TFT LCD module (right)

## 7.62-cm (3.0-in) IPS Low-temperature Polysilicon TFT LCD for Digital Still Cameras



External view of 7.62-cm (3.0-in) IPS low-temperature polysilicon TFT LCD

As digital still cameras become more sophisticated, the demand for high quality LCDs used in them is growing. To meet this demand, Hitachi has developed a high-definition LCD that takes advantage of the characteristics of low-temperature polysilicon TFTs (thin film transistors) and uses IPS (in-plane switching) to achieve a wide viewing angle and high color reproducibility in any direction. The screen size has a 7.62-cm (3.0-in) diagonal, which is one of the largest available. So that the LCD can be used in mobile devices, it is slightly reflective for outdoor visibility.

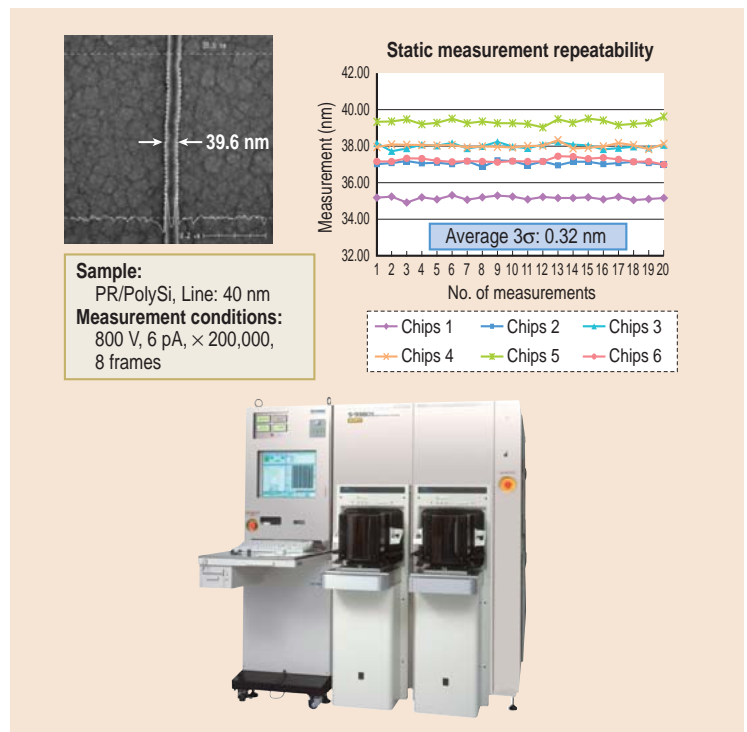
### [Main specifications]

- (1) Number of dots displayed: 960 (horizontal) × 240 (vertical)
  - (2) Display size: 7.62-cm (3.0-in) diagonal
  - (3) Viewing angle: over 170° vertically and horizontally
  - (4) Color reproducibility: 50% (ratio to NTSC standard)
  - (5) Interface: RGB 8-bit digital
- (Hitachi Displays, Ltd.)

## High-resolution FEB Measurement System (CD-SEM)

The S-9380 is Hitachi's most advanced CD-measurement SEM developed for 65 nm process control of semiconductor devices on wafers up to 300 mm in diameter. With improvement in both hardware and software, the S-9380 supports a high throughput of 33 wafers per hour with 20 measurement points per wafer, and resolution of 2.0 nm. Adjustment of the electron optics system has been automated thereby eliminating the need for a skilled operator. Measurement errors due to operator differences have been substantially reduced, and the system continues to provide highly precise CD measurements with long-term stability. The S-9380 features many refinements over earlier models including more accurate wafer alignment in auto measurement mode, measurement point addressing, auto-focusing, image recognition for detecting measurement patterns, and more. With these and other improvements, the S-9380 has achieved a new automatic measurement success rate. The system also addresses problems associated with new materials—resist shrinkage, wafer charging, and so on—and supports special application software for controlling optical doses and focusing of steppers. In addition, the system also collect 2D and 3D data for evaluating processed patterns. The S-9380 is fully compliant with international communications and safety standards, and works with GEM300 and S2-09.

(Hitachi High-Technologies Corporation)



Measured sample, static measurement repeatability (above), and appearance of the S-9380 CD-SEM (below)

## In-line Defect Review SEM for Next-generation Device Production: RS-4000 / RS-4500



In-line defect review SEM: RS-4000

Hitachi has developed the Model RS-4000 and Model RS-4500 In-line Defect Review SEMs to meet the production demands for finer next-generation devices in the 45-nm technology node and beyond. The RS-4000 performs at a high throughput of 1,200 DPH (defects per hour), which is about 3 times faster than the conventional model, and performs defect review at a high speed and high defect capture rate thereby improving image resolution (3 nm) and enhancing image processing. Combined with ADC (automatic defect classification) to identify killer defects, the tool produces data directly linked with yield enhancement in a short time. Furthermore, the newly added function of tilt image observation by tilting the electron beam enables the tool to generate more defect information. The Model RS-4500 is an enhanced tool based on the RS-4000, with the added function of intelligent automatic review point sampling for better review efficiency. When handling a vast amount of defect review data, the RS-4500 provides equivalent review efficiency to all defect sampling by sampling fewer defects.

(Hitachi High-Technologies Corporation)

## Scanning Wafer Surface Inspection System Achieves Attainable Sensitivity of 36 nm

Silicon wafers are the starting material for semiconductors, and microscopic particles and crystalline defects on the surface of silicon wafers are the primary cause of diminished yields. With continued reduction of minimum device dimensions, there is a need to detect smaller defects than 40 nm.

Using multiple photodetectors, Hitachi has now developed a scanning wafer surface inspection system that achieves an attainable sensitivity of 36 nm. The wafer transfer unit on the system has the wafer flipping function and measures contamination on the back side of the wafers, a source of contamination that has recently been implicated as problematic.

(Hitachi High-Technologies Corporation)



Wafer surface detection system

## New Silicon Etching System: U-8150



New silicon etching system: U-8150

Last year Hitachi released a new silicon etching system, the U-8150, which performs fine and accurate silicon etching on 300 mm wafers and is especially useful for gate etching after the 65 node. The U-8150 has ultra high frequency electron cyclotron resonance plasma etching technology adapted for accurate etching, which has already achieved good results, and has a new mainframe that can have four etching reactors installed. New functions have been added to the etching reactor as follows.

For fine and high-accuracy processes:

- (1) Symmetrical and high-speed exhaust system
- (2) Multiwave endpoint detector

For improved yield:

- (1) New materials for low-particle and low heavy-metal contamination etching reactor

For improved productivity:

- (1) Replaceable parts in etching reactor
- (2) Reduced inner cleaning area of etching reactor
- (3) High-speed transfer system using double-armed robot

An advanced process control system will be optional in the U-8150.

(Hitachi High-Technologies Corporation)

## Ultra-high Resolution In-lens Field Emission Scanning Electron Microscope with Scanning Transmission Electron Microscopy Capability at Low Accelerating Voltage

In the fields of electronics, materials, and biotechnology, a SEM (scanning electron microscope) is indispensable for observing ultra-fine structures. Hitachi has developed a new, ultra-high resolution in-lens FE-SEM (field emission SEM), the S-5500, with improved performance over that of its predecessor, the S-5200.

[Main features of S-5500]

(1) The world's highest resolution, 0.4 nm at 30 kV, achieved by the use of a new electron optics system (as of October 2004)

(2) New BF (bright field)/ DF (dark field) Duo STEM (scanning transmission electron microscopy) detector allows simultaneous display of BF and DF STEM images. In DF STEM mode, this detector is capable of providing images with variable detection angles. This new detection system greatly extends the usage of low accelerating voltage STEM at 30 kV.

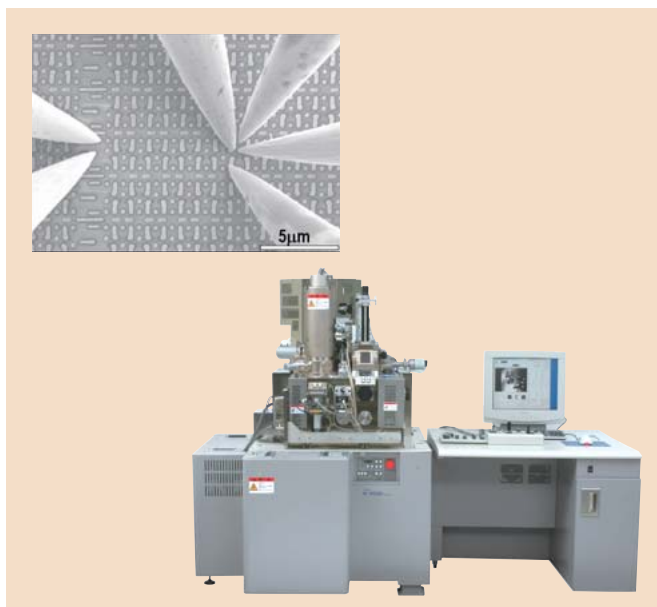
(Hitachi High-Technologies Corporation)

\* BF/DF Duo-STEM detector: option



A general view of in-lens FE-SEM, the S-5500

## Direct Evaluation of Actual Circuit on Semiconductor Device of 90 nm or Below: Model N-6000



SEM image during probing (above left) and Model N-6000 (Courtesy of Renesas Technology Corp.)

In failure analysis for semiconductor devices, logical electrical characterization is followed by physical characterization. With conventional logical electrical characterization, failed cells can be identified, but actual objects of physical analysis, failed transistors and their locations, can not be identified.

Our fine-structure device characteristic evaluation system Model N-6000, which was co-developed by Renesas Technology Corp. and Hitachi, Ltd., has six tungsten manipulation-probes mounted on SEM (scanning electron microscope), each of which has a point with a 50-nm radius. Manipulation-probes on Model N-6000 can directly touch the contacts that lead to components of transistors: source, drain, gate, substrate, etc. Model N-6000 can directly measure metal-oxide semiconductor characteristics, like small current leaks, threshold voltage shifts, contact resistances, etc.

Model N-6000 makes a bridge between logical electrical characterization and physical characterization, and helps failure locations to be identified. It dramatically improves the efficiency of failure analysis.

(Hitachi High-Technologies Corporation)