

Micro-fabrication and High-productivity Etching System for 65-nm Node and Beyond

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OVERVIEW: In regard to cutting-edge semiconductor devices, mass production of 65-nm node devices is about to begin, and development aiming beyond the 45-nm node has already started. Along with this trend, demands for advanced miniaturization and precision-improvement techniques are growing, and the needs for handling new materials and establishing production stability are getting stronger. With these circumstances in mind and taking miniaturization, high precision, and high throughput as a base concept, Hitachi High-Technologies Corporation has developed etching systems and processes for handling the post-65-nm node. Aimed at improving the uniformity across a wafer surface during etching of 300-mm-diameter wafers, an etching reactor—with uniformized discharge-gas rate and a mechanism for controlling electrode-temperature difference—was developed. A “resist trimming” technique, which can handle dimensions that surpass the exposure limit of current lithography, was also developed. Moreover, the etching reactor was designed and developed to realize low CoO, namely, improved operability and shorter maintenance downtime, and is targeting silicon-etching systems for handling the post-45-nm node.

INTRODUCTION

IN regard to semiconductor-device manufacturers, development aimed at mass production of 65-nm node devices is progressing. Accordingly, in 2006, production of 65-nm-node wafers with 300-mm diameter has started. In addition, development of 45-nm-node devices has already started. According to the

ITRS (International Technology Roadmap for Semiconductors),⁽¹⁾ the physical gate length in an MPU (micro-processor unit) is forecast to reach 25 nm for the 65-nm node and 18 nm for the 45-nm node. Feature sizes of this scale, however, surpass the limit of conventional lithography. Regarding gate fabrication in particular, aimed at speeding up transistors, new

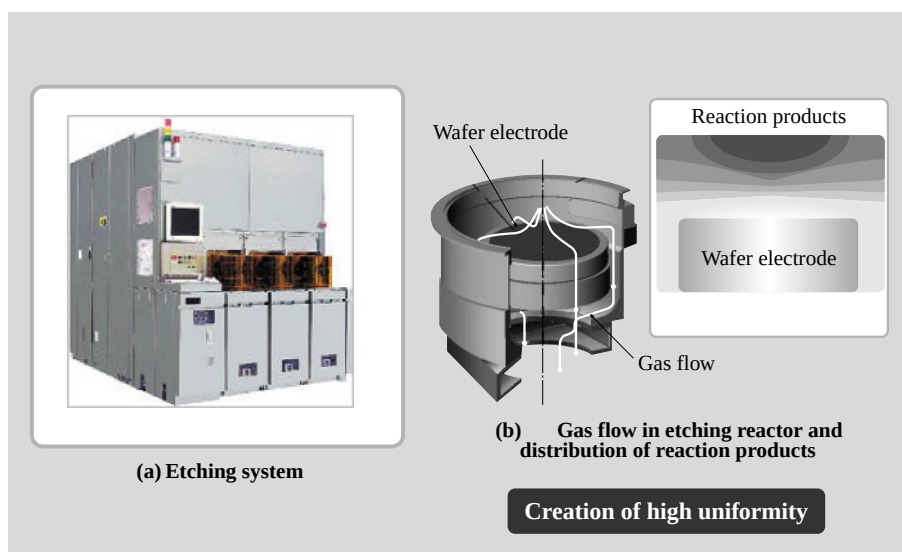


Fig. 1—Gas Flow Within Etching Reactor Fitted with a 300-mm-wafer Etching Device and Discharge Pump Directly below Electrode, and Uniformity Of Reaction Products. Hitachi's etching system (a) fitted with an etching reactor with a TMP (turbo molecular pump) directly below the electrode. By increasing the effective discharge rate, these devices can create large optimized flow rate and low-pressure plasma for miniaturization, and make uniform etching possible by forming axially symmetric reaction products.

fabrication processes and materials—namely, strained silicon for increasing channel mobility⁽²⁾, high- k gate-dielectric materials for low power consumption, and metal gate electrodes—are being developed. As regards the etching process, according to the ITRS, the fabrication process for gate lengths of less than 25 nm must have an accuracy (i.e. 3σ -distribution) of less than 1 nm. This means that even more advanced microfabrication techniques, such as photoresist trimming⁽³⁾, and materials technologies^(4–7), are being demanded. And in the case of 300-mm-diameter wafers, uniformity of the wafer surface is becoming a serious problem. On top of that, the demand for reproducibility of process dimensions is becoming ever more severe. As a result, stable etching characteristics—in and between lots as well as before and after cleaning—are also required.

With satisfying the above-described requirements as our goal, Hitachi High-Technologies is offering etching systems aimed at device mass production of 300-mm-diameter wafers for the 65-nm node and beyond (see Fig. 1). In particular, they are compatible with silicon-etching equipment and metal-etching equipment for aluminum interconnections.

The rest of this paper outlines process technologies that meet the technical demands coming from the cutting-edge-device market while satisfying our customers' needs, and describes silicon-etching equipment aimed at improving mass produceability.

TECHNIQUE FOR IMPROVING ETCHING UNIFORMITY

Creating Uniformity by Discharge Directly below Electrode

An outline of the etching reactor is shown in Fig. 2. In this reactor configuration, the discharge pump is positioned directly below the wafer electrode, and the shape of the gate valve (for feeding the reactor and wafer) is designed to have high axial symmetry.

Simulation results of the flow of the etching gas used in the reactor are shown in Fig. 3. The distributions of etchant and reactant products generated by discharge during etching show no deviations, and across the wafer surface, axial symmetry and uniformity are obtained. As a result, the surface axial symmetry of the etching shape is improved and high uniformity is obtained.

Technique for Controlling Wafer Temperature

Wafer temperature is a key parameter in determining the shape formed by etching. For example,

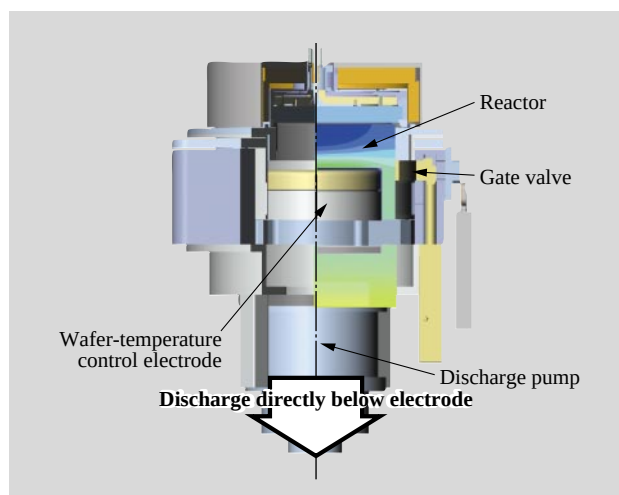


Fig. 2—Cross Section of Etching Reactor.

Aiming at improving wafer surface uniformity and ease of maintenance, a new etching reactor was developed by designing a discharge pump directly below the electrode and making parts “swap kit” type.

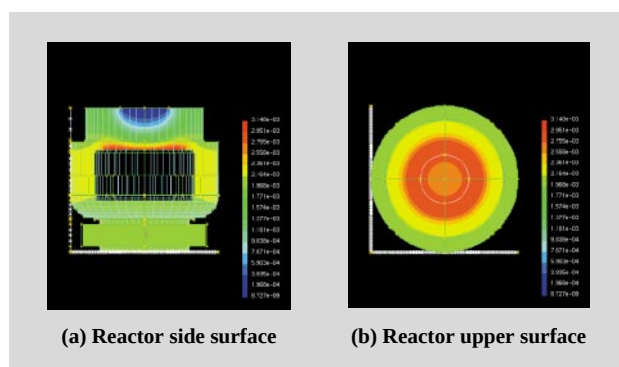


Fig. 3—Example Simulation of Gas Flow.

By realtime simulation of gas flow under conditions of 200-sccm (standard cubic centimeters/minute) chlorine-gas flow rate and reactor pressure of 0.4 Pa, it is shown that the gas-flow distribution on the reactor surface is concentrically symmetric.

even if surface temperature of a wafer is made uniform, the reaction products formed during etching are distributed in the reactor, so the final etching shape is also distributed across the wafer surface (see Fig. 4). And as for the etching film of a laminated structure, the distribution is different for each film. The distribution of reaction products in particular, becomes thinner at the periphery than at the center of the reactor, and the CD (critical dimension) shift of the etching shape is bigger at the wafer center than at the wafer periphery. As countermeasures to control these shape and dimension distributions, a temperature-control electrode mechanism for ensuring uniformity of shape

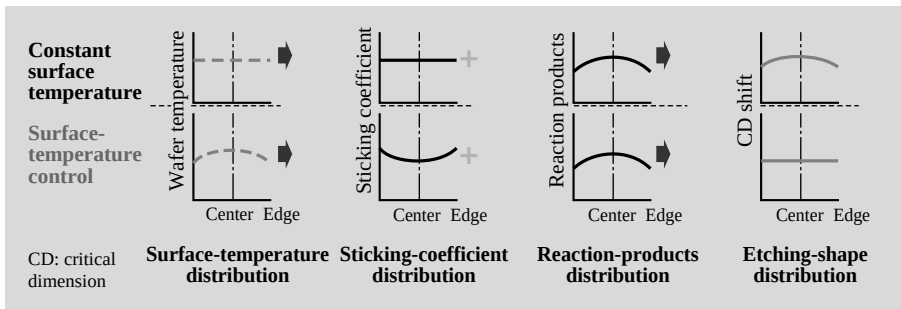


Fig. 4—Concept of Etching-shape Distribution Due to Wafer Surface Temperature.

Surface distribution of etching shape depends on temperature distribution on the wafer surface and substances in vapor phase.

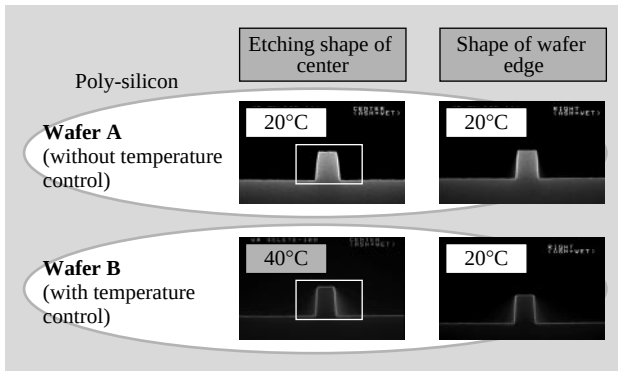


Fig. 5—Examples of Poly-silicon Etching Shape during Temperature Control of Wafer Central Part.

By raising the temperature of the central part of the wafer from 20°C (wafer A) to 40°C (wafer B), the etching-shape dimensions of the central part can be kept close those of the wafer edge, thereby improving the uniformity of the wafer surface.

across the wafer surface—that is, by independently controlling the temperatures at the center and the edge of the wafer during etching—was developed. The results of applying this mechanism are shown in Fig. 5.

At first, with temperature of the wafer periphery kept constant, poly-silicon etching under two temperatures at the wafer center was performed. In the case of wafer A (with constant temperature across the surface), the center of the wafer has a higher concentration of reaction products, and the etching shape at the center is tapered compared with that at the periphery (with low concentration). In the case of wafer B (where the temperature at the center was increased to 40°C), reattachment of reaction products to the etched central area was decreased and the vertical nature was improved. That is to say, high processing precision across the wafer surface—namely, 3 σ -distribution (CD bias) of 2 nm—was obtained. In addition, since these surface temperatures have an optimum temperature distribution depending on the process materials, an electrode structure that can

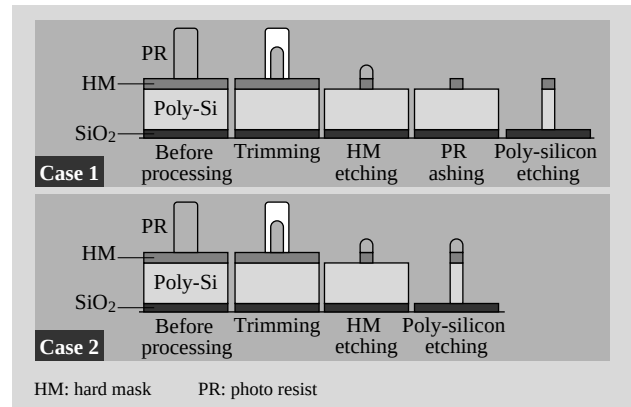


Fig. 6—Examples of Gate-etching Flow (Including Resist Trimming).

The gate-etching flow (including resist trimming) is different with or without ashing.

control wafer-temperature distribution corresponding to process materials was developed.

RESIST-TRIMMING TECHNIQUE

ArF (193-nm wavelength) lithography and its corresponding materials have been set up for mass production and are starting to be applied for the 65-nm-node process. Moreover, ArF immersion lithography tools have started to appear, and lithography techniques are improving. Many problems, however, such as ensuring the necessary gate-length dimensions obtained by 65-nm-node lithography and controlling LER (line-edge roughness), must be addressed. Accordingly, as regards handling mass production of the 65-nm-node process, controlling gate dimensions by etching and suppressing variation of gate length are the dominating techniques. Under these circumstances, as a process for handling miniature gate lengths in the 65-nm-node process and beyond, “resist trimming” was developed.

Examples of the process flow of resist trimming are shown in Fig. 6. In case 1, first, the resist

Fig. 7—Time Dependence of Resist Trimming.
Poly-silicon etching dimensions show a linearly proportional relationship with resist-trimming time; thus, the trimming amount can be controlled according to time.

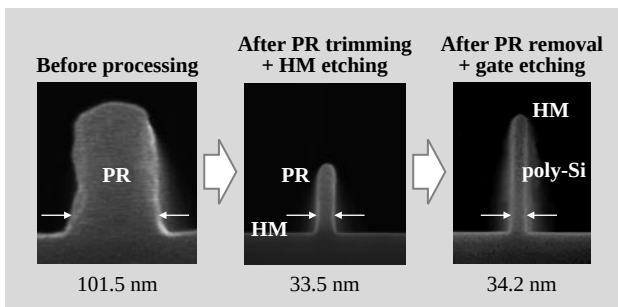
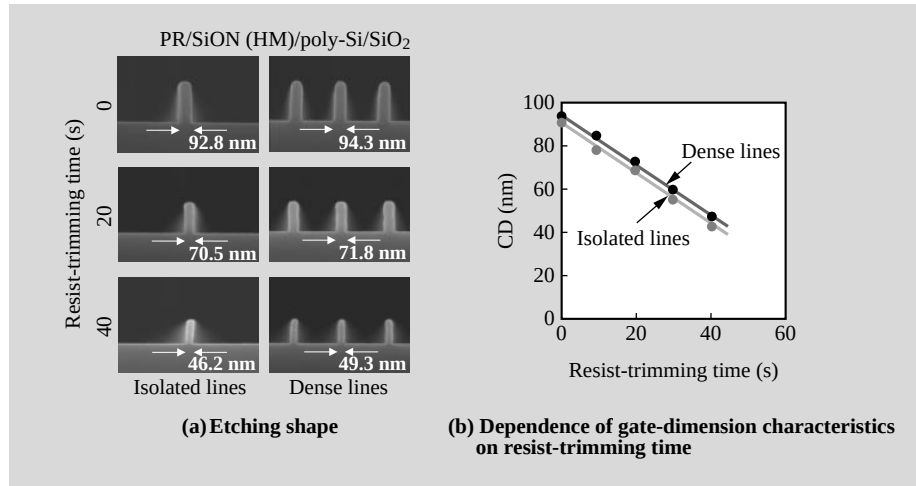


Fig. 8—35-nm Poly-silicon Gate Shape Formed by Resist Trimming.
When the case 1 etching flow (see Fig. 6) is used, an initial resist-pattern dimension of 101.5 nm can be processed to a gate-electrode dimension of 34.2 nm.

dimensions obtained by ArF are “trimmed” by etching to the required 35 nm, etching of the hard mask and subsequent ashing are performed, and the poly-silicon of the gate electrode is etched vertically. In case 2, after the same resist trimming as in case 1, with the remaining resist as is, the poly-silicon is etched.

The characteristics of poly-silicon etching while the trimming amount is under time control are shown in Fig. 7. This figure shows that the trimming amount has a linearly proportional relationship with time (a), and that trimming that produces little difference between the dimensional shape of the isolated and dense lines is possible (b).

An example of a 35-nm poly-silicon gate shape formed by resist trimming is shown in Fig. 8. After trimming down of the target resist (with a lithography-processed dimension of 100 nm) to 35 nm, the poly-silicon is vertically etched as shown in case 1 in Fig. 6. According to these results, it is clear that miniature gate-electrode processing that accommodates the limit on ArF lithography is possible.

NEW ETCHING REACTOR EMPHASIZING PRODUCTIVITY

While improving device performance by further scaling down and precision improvement, semiconductor-device manufacturers are putting a premium on increasing production volumes and decreasing costs. In accordance with that, etching devices developed from now onwards must provide stable production volume and low CoO (cost of ownership). For stable production, by composing the parts inside the etching reactor of materials with strong resistance to the plasma and by monitoring the etching conditions in real time by APC (advanced process control) systems⁽⁸⁾, it is possible to provide an extremely stable etching environment. As regards lowering CoO, in addition to the above-described points, shortening the downtime of etching equipment needed for maintenance has a significant effect.

The analysis flow for the etching reactor is shown in Fig. 9. Each part inside the reactor (such as the quartz plate) can be disassembled and cleaned. Moreover, by

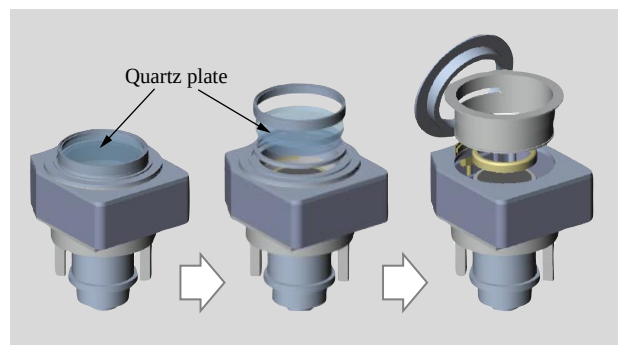


Fig. 9—Analysis Flow of Etching Reactor.
Each part (such as a quartz plate) is disassembled and replaced with spare parts, thereby improving operability and dramatically shortening maintenance downtime.

exchanging spare parts prepared in advance (known as “swapping”), operability is improved and maintenance time is shortened. Furthermore, in regards to maintenance downtime, it is possible to clean just the reactor parts in open air. At that time, in another reactor in the same etching apparatus, continuous etching processing is possible. By making 70% of reactor parts swappable, with this new reactor configuration, maintenance time per reactor can be cut by 50% in comparison with that for a conventional reactor. To sum up, as a result of this reactor configuration, productivity can be improved dramatically.

CONCLUSIONS

This paper described a silicon-etching system that attains high precision and high productivity in response to the scaling down of processes beyond the 65-nm node. The commercialized system is achieving worthy results both domestically and internationally. Moreover, our APC system—aimed at making etching equipment “intelligent”—has already been installed at some customers’ plants and is continuing to perform well. From now onwards, as process scaling-down

continues, the demands on silicon etching will get tougher and tougher, and it will be necessary to apply etching to semiconductor devices covering many types and multiple generations. In accordance with these demands, Hitachi High-Technologies Corporation will continue development aimed at upgrading and expanding high-precision silicon-etching equipment for handling further scaling-down of semiconductors and new materials thereof while improving sensing technologies for APC systems.

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