The Challenge to New Metrology World by CD-SEM and Design

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OVERVIEW: In the case of semiconductor processes, whose refinement continues at an ever faster pace, starting up a new process smoothly has become a critical point directly related to the very survival of a business. To refine a semiconductor process, semiconductor manufacturers are implementing various measures, one of which is “aggressive OPC.” For timely execution of calibration and verification by aggressive OPC, it is necessary to use a data flow that is dissimilar to that used in rule-based OPC up till now. Playing a key role in this new flow is “DesignGauge” featured in Hitachi’s design-based metrology system. Furthermore, using DesignGauge makes it possible to provide contour data extracted by the algorithms used in CD-SEM and measurement methods hitherto not available.

INTRODUCTION

As the market for semiconductor devices continues to demand higher speed and finer integration, semiconductor-fabrication processes become more and more refined. Under such circumstances, in regard to the lithography process, the demand for increased refinement has been satisfied by shortening wavelength of exposure devices, creating lenses with hyper NA (numerical aperture), and introducing low-$k_1$ factor. However, it has become a problem that patterns that differ vastly from the master shape are formed because of the use of low-$k_1$ factor. This phenomenon is known as the OPE (optical proximity effect). As a way to avoid OPE, a technique known as OPC (optical proximity correction), which superimposes a correction pattern on the master pattern, is applied. Regarding the refined processes of recent years, the OPC pattern has become more important and more complicated. Accordingly, upon controlling the yield of semiconductor processes, the need to visualize and control complicated OPC patterns is arising (see Fig. 1).

On the other hand, as for measurement technology for line thickness and so on of semiconductor devices, the mainstream technology (which had used light up till 1984) switched to measurement using an electron beam [i.e. CD-SEM (critical dimension scanning electron microscope)]. Since then, measurement by CD-SEM has been improved from year to year in terms of measurement reproducibility and throughput in line with the demands of semiconductor-device manufacturers. In the last few years, however, measurement by the conventional method for “visualization of complicated OPC” has reached a limitation. In light of this limitation, a way to apply design data (which is distinct from the conventional measurement method) has been found, and it —
Example of Applying the Fine-matching Algorithm

As for a FEM (focus exposure matrix) wafer (on which the pattern shape varies greatly), an example of determining a standard CD-SEM recipe (i.e. an image-based template), by changing the conditions of focus and exposure, is shown in Fig. 4.

Although a recipe referenced to the chip at the wafer center is created, on the chip shown by hatching in the right half of the wafer, the variation of feature sizes is significant, a pattern dissimilar from the reference pattern is recognized, but measurement is not

**Table: L/S sample**

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**Fig. 3—Algorithm for “Fine Matching.”**

An edge extracted from the design layout and SEM image is used to perform matching.

**Fig. 4—Example of Measurement by IBT.**

For a FEM (focus exposure matrix) wafer (whose shape change is significant), in regard to the measurement points on the right half of the chip, it is judged that there is no measurement target.
performed. On the other hand, for the same wafer, an example of measurement (i.e. a design-based template) by DesignGauge — loaded with the fine-matching algorithm — is shown in Fig. 5. The area that could not be measured with standard CD-SEM recipe is included, and measurement over the whole wafer becomes possible. An example showing the high robustness of the matching algorithm of DesignGauge is given in the figure.

**NEW MEASUREMENT METHOD**

**Method of Detecting Ghost Patterns**

As one means of handling processes for refinement, a technique called SRAF (sub-resolution assist feature) is well known. However, in some cases, the pattern of SRAF exerts a negative influence, and a phenomenon called a “ghost pattern” appears. From hereafter, a method for detecting ghost patterns is described. A key application for detecting this ghost pattern is EPE (edge placement error) measurement.

EPE measurement is a function for measuring the difference between the design data and the actual pattern. A measurement method applying EPE is shown in Fig. 6. By prescribing the zero line in the figure, in the case that a ghost pattern occurs, it can be detected as a positive measurement value.

**Measurement-based Contouring**

In regard to the latest lithography, the shift towards “aggressive OPC” as a more powerful OPC technique is continuing. To exploit aggressive OPC to the full, a data flow that is dissimilar to that used in conventional, rule-based OPC is necessary. Given that necessity, the data called “contour data” is a promising candidate (see Fig. 7).

To correctly execute calibration by OPC, however, it is necessary to apply the measurement algorithm adopted in conventional width measurement, etc. without change and OPC must also perform calibration according to conventional process-control rules. Given that need, we have developed a contour-extraction function called “measurement-based contour” incorporating the measurement algorithm used in CD-
Fig. 8—Extraction Algorithm of Measurement-based Contouring.

Contour data extracted from the same measurement algorithm as that of CD-SEM is effective for aggressive OPC.

SEM. The contour-extraction procedure consists of the three steps listed below (see Fig. 8).

1) An image based contour is extracted by image processing from a SEM image.
2) Edges are detected by the measurement algorithm as CD-SEM.
3) The line extracted in step 2 is transformed to GDS (graphic data system).

CONCLUSIONS

DesignGauge described in this report is an effective system product that fully utilizes the functions of CD-SEM. In the case of semiconductor processes (whose refinement will hereafter continue at an ever faster pace), applying DesignGauge will contribute to improvement of the accuracy of aggressive OPC (one technique considered to be of paramount importance) and speeding up of OPC calibration. Moreover, even in the case that the exposure conditions of SRAF (one of the latest lithography techniques) are optimized, by using EPE measurement (which is not used in conventional measurement techniques), it is possible to reliably narrow down the exposure conditions. In addition, in regard to production processes, using a highly robust matching algorithm with design data and considerably improving the automation ratio of the measurement recipe in a short time will go a long way toward achieving “vertical startup” (i.e. attainment of full production immediately) of processes. Through applications using DesignGauge — provided by Hitachi High-Technologies Corporation — the techniques described here will lead to a new paradigm for measurement technology.

REFERENCES


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