# Hitachi Releases the embedded DRAM ASIC "HDL5K Series" - "HDL5K Series" with maximum 144-Mbit ultra high-speed DRAMs operating at the world's fastest speed of 700 MHz is to be launched for sale -

Tokyo, June 3rd, 2003 - Hitachi Ltd.,(TSE:6501,NYSE:HIT) today announced the embedded DRAM ASIC "HDL5K Series" with maximum 144-Mbit ultra high-speed DRAMs operating at the world's fastest speed of 700 MHz. The new series will be released on the 5th of June. Using the CMOS (complementary metal-oxide semiconductor) process, the new series will offer a large-capacity DRAM that ensures a high operating speed of 700 MHz, almost equivalent to that of the SRAM in ASIC(\*1). The new series will ensure high-speed processing for cache memories (\*2) for high-performance servers or buffer memories for routers and switches in networking systems, or high-performance graphic engines for PCs and car navigation systems.

(\*1) ASIC (Application Specific Integrated Circuit): An application-specific customized IC.

(\*2) Cache memory: A high-speed memory located between the microprocessor and main memory. It is used to improve server performance by storing frequently-used data and reducing access to the slow-speed main memory.

Together with the advance of an information-networking society, broadband networks that cope with the increasing information capacity and speeds have been rapidly expanding. When designing products such as servers and networking equipment for broadband networks, PCs and car navigation systems, devices that are capable of rapidly processing staggering volumes of information at high speeds are much sought after.

The new series was developed by Hitachi's Device Development Center, being based on the "High-Speed Large-Capacity Cache DRAM LSI Technology" presented in the "2003 International Solid-State Circuits Conference" held February 9, 2003, in San Francisco, U.S.A. To meet varied users' needs, the new series can be customized with a diversified range of capacity and speeds. During the design process, we provide support for customers to shorten lead times, such as sharing operations in designing with the customers and providing high-precision DA tools for development and tests.

## - Major features of the "HDL5K Series"

## 1. Ultra high-speed DRAM and high-speed logic are integrated on a single chip

Maximum 144-Mbit DRAMs operating at 700 MHz can be mounted. With its peak memory band (\*3) at 81 GB/sec., it is most suitable for products requiring high-speed operation.

## 2. Customization according to users' specifications

By customizing the memory capacity of chips and processing speed, the new series offers products to meet users' specifications with high cost performance.

## 3. High testability with "At speed DRAM BIST (\*4)" and Logic BIST

The on-chip programmable test pattern generator that reproduces actual data pattern on user's system is introduced to expose subtle faults in embedded DRAM arrays and the interface between DRAM and logic, thus realizing high reliability on system operation.

(\*3) Peak memory band: An index to indicate the speed with which data is read and written at its peak level. (\*4) BIST (Built-in Self-test): Diagnostic function test technique by which testing is accomplished through built-in test circuit on the LSI.

Items		High-density type	High-speed type
		HD(High Density)	HS(High Speed)
Random access time		20ns (*5)	9.5ns
Page access time		6.3ns	6.3ns
Random cycle time		32ns	15.8ns
Maximum operating frequency		700MHz (*6)	
Memory density	without parity (*8)	8Mb / 16Mbit (*7)	
	with parity	9Mb / 18Mbit	
IO width	without parity	128 / 256	
	with parity	144 / 288	
Macro size	9Mbit	8.5mm <sup>2</sup>	9.9mm <sup>2</sup>
	18Mbit	14.5mm <sup>2</sup>	19.1mm <sup>2</sup>

## - Specifications of the embedded DRAM ASIC "HDL5K Series"

(\*5) ns (nano second): One-billionth of a second

(\*6) MHz (mega Hertz): One million Hertz

(\*7) Mbit (mega bit): One million bits

(\*8) Parity: A bit to detect a data error. One parity bit is built-in for each 8-bit data.

#### - Price and delivery

Product name	Standard price	shipment availability
HDL5K series	Individual estimate	October 1st, 2003

## - Home page for product information

http://www.hitachi.co.jp/Div/ddc/english/product/product.html

## - Indication about other companies' trademarks

The described company names and product names are trademarks or registered trademarks of the respective companies.

## - About the Device Development Center

The Device Development Center is developing and producing cutting-edge LSIs for such information and communications equipment as storage systems, hard disks, server systems and networking devices. Its activities include not only the development of semiconductor-related cutting-edge technology and commissioned production of LSIs and wafers for the Hitachi group companies, but also semiconductor production and foundry business for non-group customers.

#### - References

Person in charge: Kojima Planning Office, Device Development Center, Information and Telecommunication Systems, Hitachi, Ltd. 6-16-3, Shinmachi, Ome-shi, Tokyo 198-8512 +81-428-33-2011 (direct dialing) Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.

\_\_\_\_\_