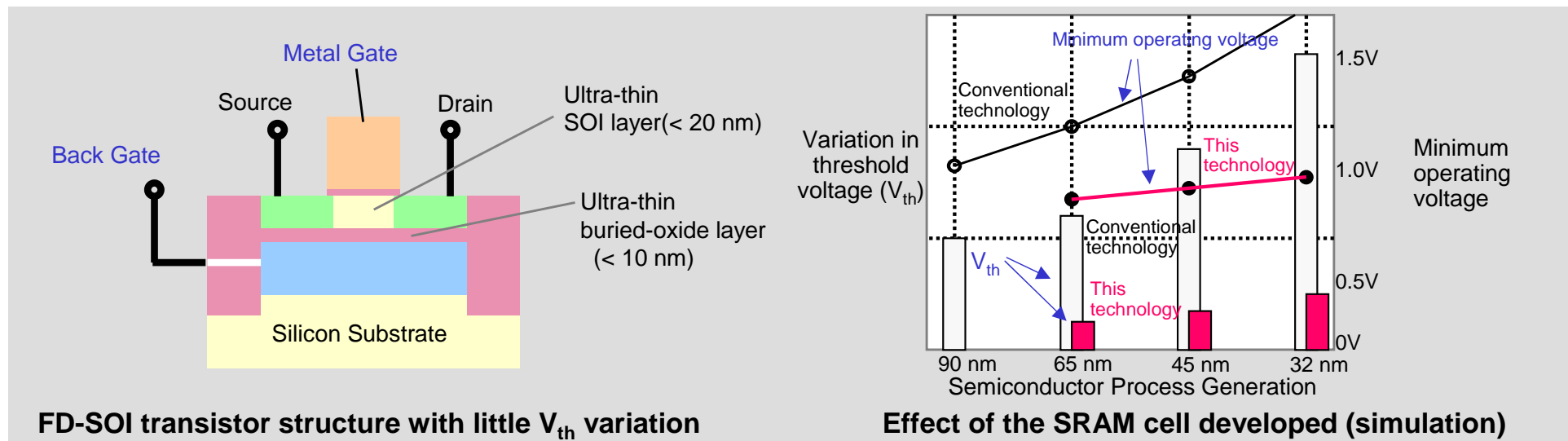


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Development of a four-transistor-type SRAM cell using double-gate FD-SOI transistor - Reducing leakage current by 1/1,000 and enabling embedding in SoC -



FD-SOI transistor structure with little V_{th} variation

Effect of the SRAM cell developed (simulation)

The Central Research Laboratory of Hitachi, Ltd., has designed a new small-area low-power SRAM cell, suitable for SoC (System-on-a-Chip) used in mobile devices, and has verified its effectiveness by simulation. The new SRAM cell is composed of four FD-SOI*1 (Fully-Depleted Silicon-On-Insulator) transistors, with a double-gate structure. The standby leakage current is about 1/1,000 compared to a conventional four-transistor memory cell. This technology enables a small-area high-density four-transistor SRAM cell to be embedded into a low-power SoC.

These results were presented at the Symposium on VLSI Circuits, held in Hawaii, U.S.A. from 17th-19th June 2004.