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Hitachi, Ltd.

Development of the world's fastest 20-nm Gate-length CMOS Technology
- One-order reduction of leak current with a nitride-based gate insulator -

Hitachi Ltd. (President: Mr. SHOYAMA Etsuhiko) has developed a 20-nm gate-length CMOS (Complementary Metal Oxide Semiconductor) device technology suitable for high-speed, low power applications. The world's fastest device operation speed was achieved, as well as reduction of gate leakage current to less than one-tenth of previous levels, by further scaling of the gate length and the development of a nitride-based gate insulation film. This result will contribute as key technology for next-generation high-speed low power CMOS suitable for th e expanding mobile equipment market.

The progress of system LSI performance, which can be said to be the heart of mobile equipment, has opened doors to increasing the functionality of mobile equipment and is sustaining a rapidly expanding market. System LSI performance is measured by factors such as high-speed as well as low power consumption which defines the battery life of mobile equipment. CMOS devices, used in system LSIs, have achieved these improvements by decreasing the scale of the gate-length and thinning of the gate insulation film. However, while thinning of the insulation film does contribute to increased speed, at the same time it detracts from its function as an insulator, leading to greater power consumption due to leakage current. In the 0.1 micro-meter generation, this problem becomes even more evident. Thus the development of a CMOS device achieving high-speed performance while controlling gate leakage current was indispensable.

The Central Research Laboratory and Device Development Center, both of Hitachi, Ltd., co-operated to develop CMOS technology providing excellent low voltage and high-speed performance.

Features of the new technology developed are as follows:

(1) Optimisation of gate fabrication process and reduction of gate capacitance for high-speed operation: A gate length of 20nm was realized by adding a process of "trimming" to the gate fabrication process. Further, to increase transistor operation speed, it is necessary to decrease gate capacitance, which controls the on and off current, at the same time. An offset-spacer structure[*1] was employed to reduce gate capacitance, and high-speed operation realized.

(2) Nitride-based gate insulator film which inhibits gate leakage current: An ultra-thin nitride-based gate insulator was developed using an original Hitachi technique for film formation where oxygen is incorporated during the nitride layer formation. This insulation film has a high dielectric constant[*2] compared to previous film, and is thus able to inhibit gate-leakage current. Further, from the viewpoint of transistor performance, it has the advantage of providing high dielectric constant characteristics, as it can be formed maintaining an excellent interface between the insulation layer and the silicon substrate,

The prototype CMOS device has a gate-length of 20-nm and a gate insulation layer of 1.4-nm. When the operation performance of the 20-nm gate-length CMOS device was measured, a result of 280 femtoseconds, the fastest in the world, was achieved. Further, it was found that gate leakage current was reduced to less than one order of magnitude compared to previous devices

with the same gate insulator thickness. Furthermore, it was confirmed that the transistor output current was increased to approx. 7% in the n-channel, and 20% in the p-channel. As further thinning of the nitride-based gate insulator is possible, indicating that even higher performance devices can be achieved. This technology will be further developed as key technology for high-speed low-power CMOS, a necessity for highly functional mobile equipment.

This research result will be presented at the “2002 Symposium on VLSI Technology", an international conference on the electronic device, to be held in Honolulu, U.S.A. from 11th June 2002.

■Explanation of Terms

1) Offset-Spacer Structure: A structure to reduce the gate region by lining the side wall of the gate with an insulation layer.
2) The larger the dielectric constant, the greater the charge can be stored, having the effect of inhibiting gate leakage current from the gate insulator.

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