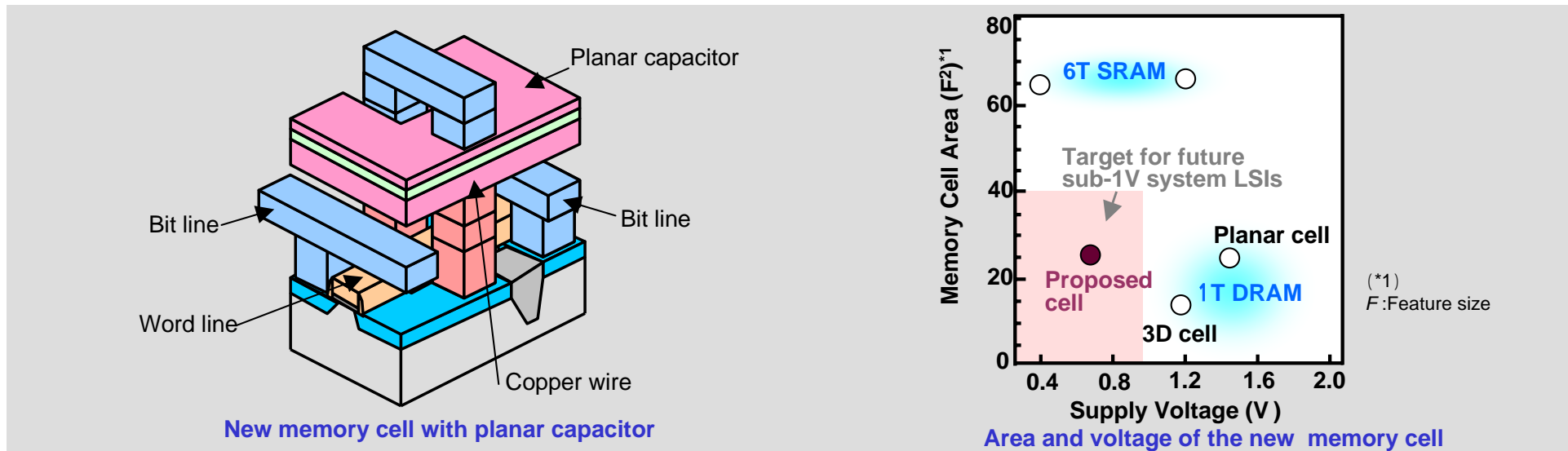


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## A 0.72V SoC memory cell with 40% the area of SRAM proposed - A high density, low voltage embedded memory solution -



The Central Research Laboratory of Hitachi, Ltd. (General Manager: Dr. NISHINO Toshikazu) has proposed a new on-chip memory cell achieving higher density and lower voltage operation at the same time. The memory cell, fabricated by the addition of a single photo mask in the CMOS<sup>(1)</sup> logic process, operates at 0.72V and occupies 40% the area of standard SRAMs<sup>(2)</sup>.

The proposed memory cell consists of two transistors combined with a planar capacitor formed over copper wiring and introduces a large capacity embedded memory for future sub-1V system LSIs.

- Note: (1) CMOS: Complimentary Metal Oxide Semiconductor  
(2) SRAM: Static Random Access Memory