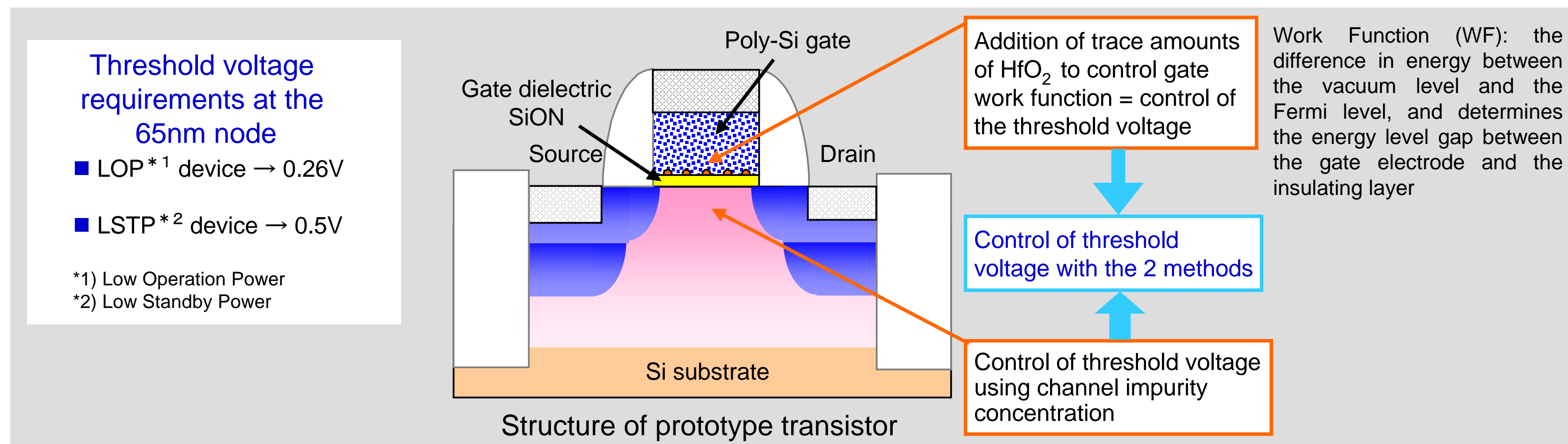
2005/6/15 Release

Gate insulator fabrication technology for high-speed low-power CMOS beyond the 65nm node

- Improved carrier mobility and decreased leakage current achieved with addition of hafnium -



Structure of prototype transistor

Hitachi, Ltd., in collaboration with Renesas Technologies Corp., have developed gate dielectric fabrication technology to achieve high-speed low-power CMOS (Complementary Metal-Oxide Semiconductor) beyond the 65 nanometer (nm) node. This technology adds a trace amount of hafnium to the interface between the gate dielectric and the gate electrode, to attain increased carrier mobility and decreased leakage current. Having a high compatibility with conventional CMOS transistor fabrication methods, it is expected to become fundamental technology in achieving low-power CMOS beyond the 65 nm node.

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