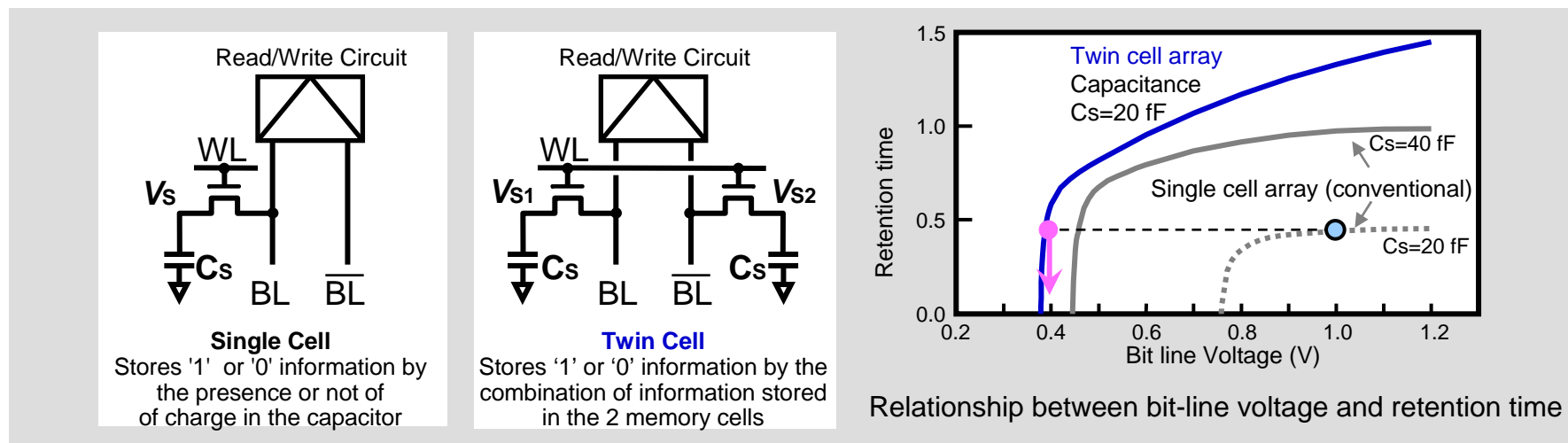


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0.4V DRAM array technology using twin cells for next-generation mobile devices - Enabling longer retention time and fast read/write operation under low voltage condition -



Hitachi, Ltd., in cooperation with Elpida Memory, Inc., have proposed a new DRAM circuit design enabling 0.4V operation. The proposed array employs a twin cell scheme, which uses two conventional DRAM cells to store 1-bit information, and achieves a longer retention time and fast read/write operation under low voltage condition. This technology will be fundamental for designing DRAM, with its large memory capacity, as the low power memory device in next generation mobile information devices.

BL: Bit line
WL: Word-line

Cs: capacitor to store charge
fF: femto (f) – a metric prefix for 10^{-15} ; Farad (F) – a measure of capacitance.