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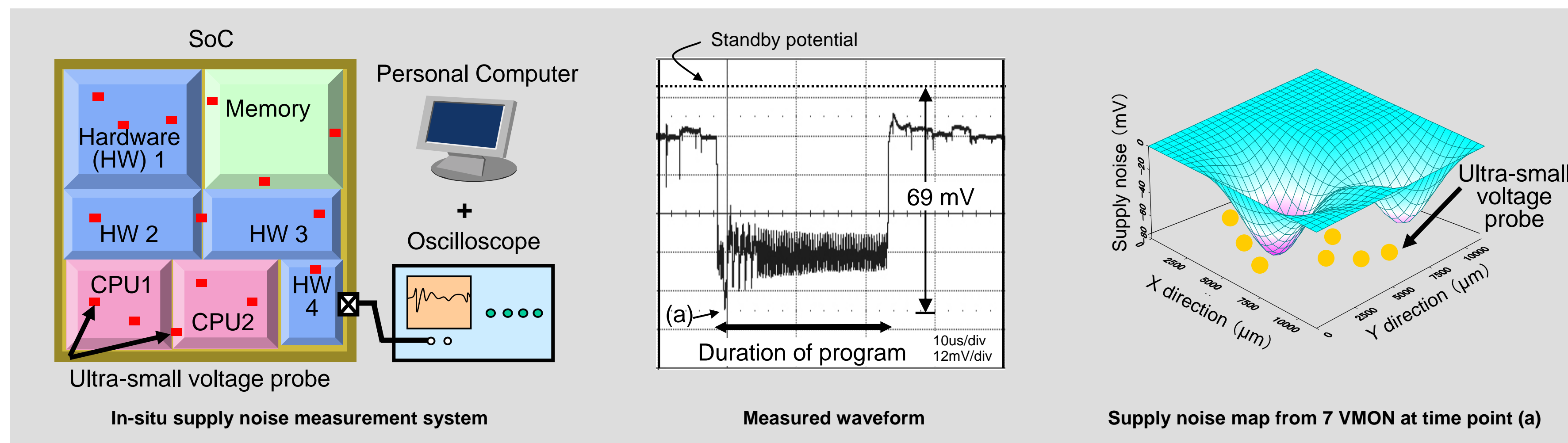
Measurement of in-situ supply noise with an accuracy of 1mV in highly integrated LSIs

- Providing design feedback to avoid performance degradation resulting from drops in supply voltage -



In-situ supply noise measurement system Measured waveform Supply noise map from 7 VMON at time point (a)

Hitachi, Ltd. and Renesas Technology Corp. have developed a technique for “in-situ measurement of supply noise” which visualizes the supply noise map within a product-level system-on-a-chip (SoC) for the 90nm process node and beyond. Multiple ultra-small voltage probe circuits within the SoC and high-resolution off-chip digital signal processing are key elements of this technique. By using this technique, an accuracy of 1mV for the supply noise measurement was achieved while the SoC is in operational mode. The supply noise becomes one of crucial problems to lead to decreased LSI performance. Therefore, by analyzing the measurement results and applying the knowledge in the design phase of the next chip, design efficiency and improved performance can be achieved.

Details of this research were presented at the 2006 Symposium on VLSI Circuits, held in Honolulu, Hawaii, U.S.A., from 15th - 17th June 2006.

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