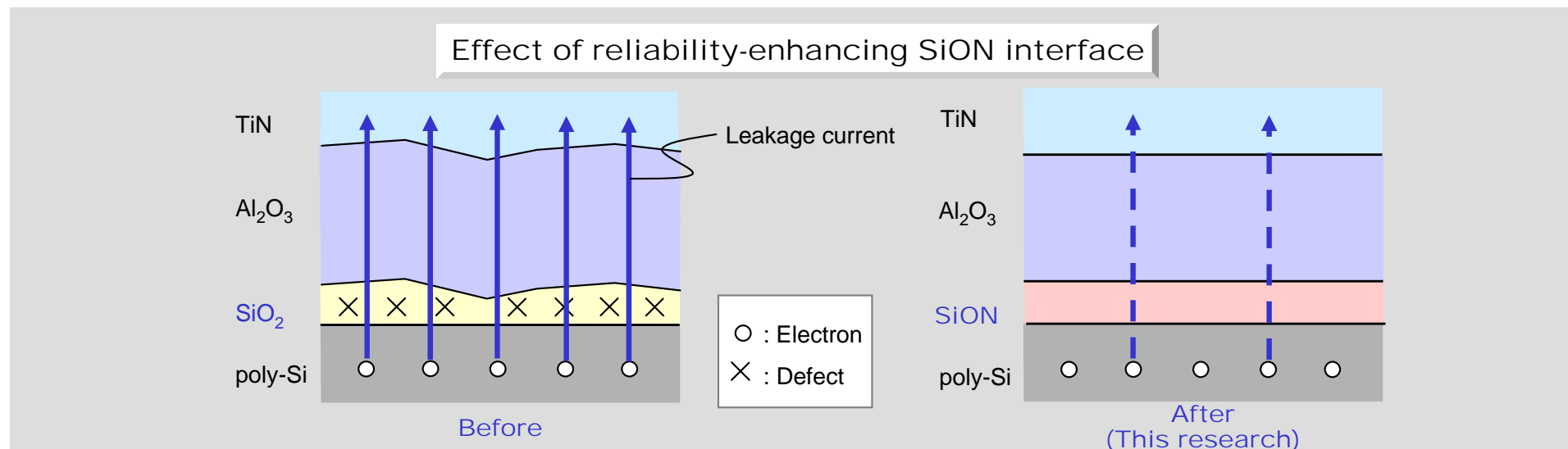


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Fundamental DRAM capacitor technology for high-throughput Al_2O_3 dielectrics fabrication and reliability-enhancing SiON interface 10% suppression of power consumption contributing to longer running time in mobile equipment



The Central Research Laboratory of Hitachi, Ltd. has developed a throughput-enhancing technique for the fabrication of a highly reliable capacitor insulating layer in DRAMs for the 90 nanometer technology node and beyond. To reduce the time required for film formation, water (H_2O) was used as one of the precursors for the deposition of the alumina insulating layer. This process was followed by ozone annealing to attain sufficiently low leakage current. Further, by using an oxynitride interfacial layer which provides an extremely flat interface between the alumina and the polysilicon lower electrode, leakage current was further reduced, contributing to an increase in capacitor reliability. As a result, in DRAMs employing this technique, power consumption can be reduced by about 10%. This result is expected to contribute to low power operation in large capacity DRAMs integrated in system-on-chips, thus extending the running time of mobile equipment.

Results of this research will be presented at the 2006 International Conference on Solid State Devices and Materials (SSDM 2006) to be held at Pacifico Yokohama, Yokohama-shi, Japan, from 13th - 15th September 2006.