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Low-power LSI technology for future low-power consumption supercomputers Program pattern based control of operating frequency and substrate voltage for power conservation

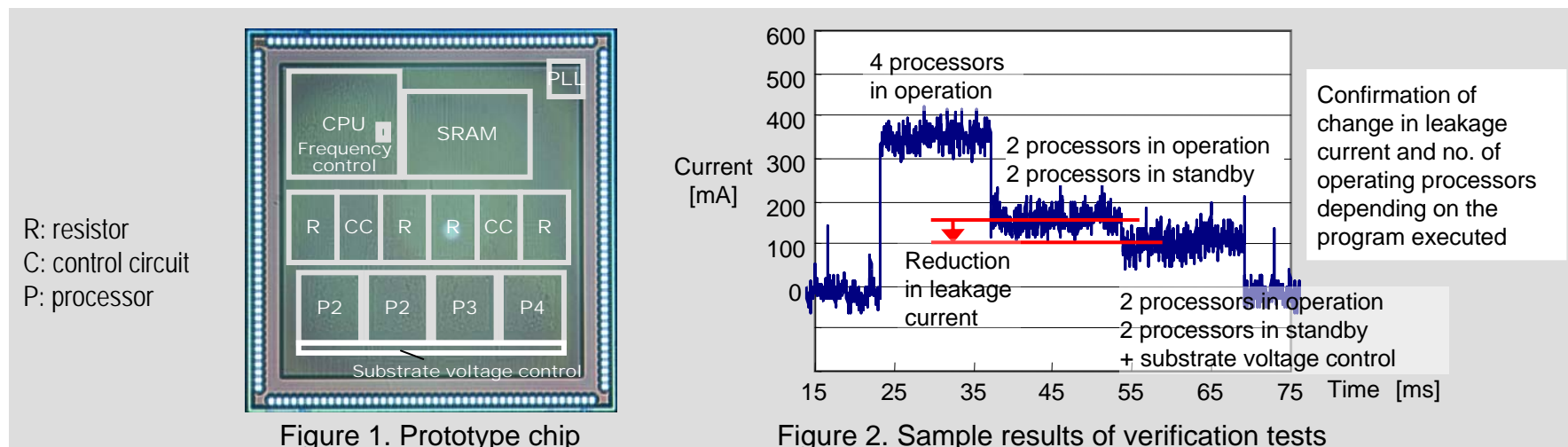


Figure 1. Prototype chip

Figure 2. Sample results of verification tests

Hitachi, Ltd. and Professor SAKURAI Takayasu of the Institute of Industrial Science of the University of Tokyo announced that by finely controlling the processors used in supercomputers, they have co-developed technology enabling the reduction in power consumption of LSIs consisting of integrated processors. This technology makes use of the ability to identify which processor is performing a calculation by program pattern during a large-scale computation on a supercomputer. By incorporating a circuit (resistor circuit) to control the processor operating frequency and substrate voltage, it is possible to lower the operating frequency of non-performing processors. Further by controlling the substrate voltage, leakage current can also be reduced, thus making it possible to save power in the LSIs as well as the supercomputer as a whole. Verification tests with this prototype chip yielded a maximum reduction in power consumption of 50%. This development achieves both high performance and low power consumption, and provides basic technology towards achieving an environment-conscious large-scale supercomputer for scientific calculations.

These results will be presented at the 2008 Symposium on VLSI Circuits, to be held in Honolulu, Hawaii, U.S.A., from 18th – 20th June 2008.

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