Semiconductor Device Technology for Implementing System Solutions: Memory Modules

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ABSTRACT: New technology is producing rapid advances toward ever higher performance semiconductor devices, including memory devices and modules. The performance of information equipment, such as personal computers and workstations, is improving dramatically with the use of the newest microprocessing units (MPU). In order to operate more-advanced larger-scale software, the necessity for larger-scale memory is driving advances in main memory capacity, while requirements are increasing for higher-speed higher-performance modules matched to new wider-width MPU buses. Using leading edge technology along with experience and know-how obtained in the semiconductor marketplace, Hitachi, Ltd. is providing a complete line of memory modules for improved versions of systems for various applications. These products flexibly and accurately support customer needs. In addition, in order to support further increases in MPU speed, development is advancing on high-capacity ultrahigh-speed synchronous dynamic random access memory (SDRAM). This product will greatly improve the performance of memory systems.

INTRODUCTION

SINCE the appearance of the 256-kbyte 30-pin single in-line memory modules (SIMM) in 1985, the size of memory modules has grown rapidly with advances in downsizing high-performance computers. A memory module consists of multiple memory chips organically mounted on a circuit board with certain specific functions. One major advantage of the module is the ability to easily expand memory capacity using the same space. This special advantage is the reason that memory modules have come into widespread use as the main memory of personal computers (PCs) and workstations (WSs).

Over the years the modules have advanced from the 30-pin SIMM to the 72-pin SIMM and the 168-pin dual in-line memory module (DIMM). However, the functions of dynamic random access memory (DRAM) have also changed from normal page mode to fast page mode, and to include extended data output (EDO) and the synchronous dynamic random access memory (SDRAM) with single data rate (SDR).

Access times have advanced from 120 ns to 100 ns to 80 ns to 60 ns to 50 ns and operating frequencies have increased from 22 MHz to 33 MHz to 66 MHz to 100 MHz. Asynchronous operation has been replaced by clock synchronization, and the input and output interfaces have progressed from 5-V transistor logic (TTL) to 3.3 V-TTL to stub-series terminated logic (SSTL). All of the above advances have provided ever higher levels of speed and performance.

Thus the data transfer rate of memory modules has increased by over 40 times from 22 Mbyte/s to 800 Mbyte/s in the past several years (Fig. 1). Accompanying these trends and in order to realize the high capabilities of the MPU, higher speeds have been demanded for data transfer on the system bus. In fact, currently even more advances in SDRAM module products and remarkably improved data transfer rates have gained attention. This report discusses the current state of memory modules and future trends.

MEMORY MODULE

Required Capabilities

Demands related to memory modules are listed below. (1) Physical specifications such as external shape and dimensions. (2) Capabilities matched to system bus; including data bus width, data transfer rate, and impedance matching. (3) Expandability of the memory section while maintaining a high standard of compatibility.

With regard to (1), an external shape concept that seriously considers system space, especially in PCs and WSs, is being established and international
standardization is occurring. The DIMM currently found most often in desktop PCs and WSs and the small outline (SO)-DIMM well accepted in portable PCs were both created by Hitachi, Ltd. In the future, demand will probably increase for thin miniature module configurations applicable to portable equipment.

With regard to (3), a standard module concept—including pin arrangement, structural memory specifications, function block diagram, and recognition codes—is being planned and international standardization is occurring simultaneously with (1). The plans take bus performance improvements into consideration along with memory expandability and compatibility. The currently leading 8-byte module concept was drafted by Hitachi, Ltd.

In the future, with high speed modules having data transfer rates exceeding 100 MHz, a consensus will probably be necessary for concrete application specifications in memory systems extending from large scale to small.

While demands for significant improvement in data transfer rates continue to mount, item (2) becomes very important and is closely related to items (1) and (3). Item (2) is also closely related to the system hardware. While it goes without saying that improvements in memory assembly design technology are required, memory system technology improvements will also be necessary.

The following areas are becoming increasingly important in memory assembly design technology.

(1) Forecasting technology for optimization of parts layout and printed circuit board (PCB) wiring layout through the use of module transfer circuit simulation.
(2) Selection method for optimization of installed parts.
(3) PCB design technology taking impedance into

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**Fig. 1—Speed and Capacity Increases in High-Capacity Ultrahigh-Speed SDRAM Modules.**

An external clock synchronized SDR-SDRAM module with increased data transfer rate to meet requirements for improved memory system performance has been marketed along with a multilayer TCP SDRAM to meet requirements for high capacity.
Development Guidelines

In addition to a central processing unit consisting of an MPU and related circuits, current PCs and WSs also contain screen display subsystems and memory systems containing chip sets. Use of memory modules in the main memory has become the general rule. Moving beyond the needs of various systems, Hitachi, Ltd. is investigating module development trends and consulting with customers to advance practical development of module products as shown in Fig. 2.

For the improvement of memory system performance, Hitachi’s rule is balance among data bus width, data transfer rate, and total memory capacity. Modules based on this rule and suited to individual systems are developed into products in a timely fashion.

The following guidelines are used in the development of memory modules. The 8-byte specification currently in primary use is the base for the data bus width of a module. In order to maintain standardization and general applicability, the individual systems of customers are checked against international standard specifications and the development trend map by application engineers at Hitachi, Ltd. With the current generation of memory the maximum memory capacity is realized by ultrahigh density assembly such as multilayer tape carrier package (TCP). Data transfer rate is improved through the installation of leading-edge memory and module assembly design technology.

In response to user needs for system performance improvements, Hitachi, Ltd. developed the SDR-SDRAM module with higher data transfer rates and external clock synchronization. In addition, a TCP multilayer SDR-SDRAM module is also marketed to meet high capacity requirements. In order to handle demands for increased speed and performance levels, development is underway for a double data rate (DDR)-SDRAM module using the clock synchronized mode and having twice the output data rate.

OUTLINE OF SDRAM MODULE

Development Background

With conventional computer systems the characteristic nature of information was used and memory was generally divided into a hierarchy of main...
memory, buffer memory, and second cache memory. The low-cost DRAM was used in large quantities in main memory, and demands for increased speed were taken care of by the specialized high-speed static RAM (SRAM) used in buffer memory and cache memory.

However, the remarkable increases in MPU capabilities have caused incredible advances in computer downsizing and software performance levels. These changes have brought about demands for higher-speed large-capacity memory. Product development of MPUs is occurring in the high operating frequency ranges and is currently at the 200-MHz level (Fig. 3).

However, the data transfer rate of DRAM is at best 22 MHz, and is only improved to 33 MHz with EDO. Therefore increased speed in the main memory is indispensable in improving the cost-performance ratio of PCs. Thus an SDRAM module compatible with a 66-MHz data bus was developed. The module uses an external clock synchronization mode and has twice the conventional data transfer rate. The new SDRAM modules were developed to provide greatly improved data transfer rates while maintaining compatibility with conventional modules.

Product Outline

The product specifications of the SDRAM module include compatibility with the pin arrangement of EDO modules and support of both modules is possible using a single chip set. In addition to increasing the number of choices available to users, these modules provide a simple upgrade for replacing EDO with SDRAM.

The specifications of the first SDRAM modules produced by Hitachi, Ltd. include a 64-bit bus width—the standard configuration in current PCs, a data bus transfer rate of 66 MHz, and use of an unbuffered interface. The product line includes a 168-pin DIMM and a 144-pin SO-DIMM, both with 16-Mbit DRAMs. Hitachi also produces 66-MHz and 100-MHz data-bus transfer rate modules with 64-bit bus width based on 64-Mbit SDRAMs.

The latest Hitachi SDRAM module products include a 100-MHz 168-pin DIMM product. The 256-Mbyte module—configured as 32 Mword × 64 and consisting of 32 units of 2 bank, 16 Mword × 4 TCP multilayer TCPs—embodies original technology developed by Hitachi, Ltd. It provides the highest capacity based on a 64-Mbit SDRAM before the emergence of next-generation SDRAM such as 256-Mbit SDRAM or 128-Mbit SDRAM. Also, 32-Mbyte, 64-Mbyte, and 128-Mbyte module products based on a 64-Mbit SDRAM are in production. These modules are currently mass produced for use as main memory and expansion memory in PC servers and desktop PCs.

Also available is a 66-MHz 144-pin SO-DIMM product. The 128-Mbyte module—configured as 16 Mword × 64 and consisting of 16 units of 1 bank, 16 Mword × 4 TCP multilayer TCPs embodies original technology developed by Hitachi, Ltd. It provides the highest capacity based on a 64-Mbit SDRAM before the emergence of the next-generation SDRAMs. Also, 16-Mbyte, 32-Mbyte and 64-Mbyte module products based on a 64-Mbit SDRAM are in production. These modules are currently mass produced for use as main memory and expansion memory in laptop PCs.

Fig. 3—High Speed Trends in Memory and MPU. MPU development is advancing in the high operating frequency range.
Hitachi, Ltd. is also marketing or preparing for mass production and marketing the following SDRAM modules for high-end machines.

1. A phase-locked loop (PLL) registered 168-pin DIMM product: This product was developed for customers using low voltage TTL (LVTTL) interfaces in applications such as PC servers with a relatively large number of modules.

2. PLL registered SSTL 168-pin DIMM product: This product, currently in preparation for mass production, is for customers requiring a high data rate bus in server applications with a large number of modules.

**MODULE DESIGN TECHNOLOGY**

**High Density Assembly Design**

In order to realize the maximum memory capacity in the memory modules of each generation, Hitachi, Ltd. developed an original TCP memory package that has only 1/2 the thickness of the standard thin small outline package (TSOP). Hitachi also established a high-density assembly technology making it possible to install an upper and lower layer on the front and back of module circuit boards while using only the TSOP mounting space.

This technology is applied in SDRAM modules and has been marketed as the HB526R864ESNK 2-bank, 64-Mbyte DIMM and the HB526R464DBC 1-bank, 32-Mbyte SO-DIMM. These modules were the first products based on 16-Mbit SDRAM before the emergence of 64-Mbit SDRAM. User reaction was exceptionally good, and new needs were effectively created.

Now Hitachi is applying the same technology to 64-Mbit SDRAM-based 256-Mbyte DIMM and 64-Mbit SDRAM-based 128-Mbyte SO-DIMM.

In the future clocks, and input capable of accommodating installation of additional memory along with application of multilayer TCP to SDRAM modules with PLL and resistors will provide memory modules with ever greater capacity.

**Circuit Simulation**

It would not be an overstatement to say that SDRAM module products were created by circuit simulation technology. In creation of product concepts for SDRAM modules, Hitachi created memory data bus frequency and module installation maximum quantity guidelines based on circuit simulation results with a system model (Fig. 4). Based on the guidelines a standardized road-map was proposed to Joint Electron Device Engineering Council (JEDEC) and standardization has advanced for various concepts. Consequently, standardization was done by JEDEC in the sequence LVTTL unbuffered followed by LVTTL registered followed by SSTL registered.

Simulation was used to determine the basic specifications for the SDRAM modules; including the required number of clock pins, clock pin memory allocation, matching resistance values for output pins, and damping resistance values for clock pins. Thus simulation has been used in all phases of design from the product concept determination phase through detailed design. In order to further increase the data rate of memory modules, simulation verification is necessary.
indispensable and improvements in simulation technology have become very important.

**NEXT-GENERATION HIGH SPEED MODULES**

Hitachi, Ltd. is planning to market a DDR-SDRAM module, with DDR-SDRAM installed, for next-generation modules for high speed data transfer in excess of 100 MHz. Compared to conventional SDRAM, which synchronizes data output at the rising edge of the clock signal, DDR-SDRAM synchronizes data output at both the rising and falling edges of the clock signal, and can realize twice the data transfer rate at the same clock frequency (Fig. 5).
DDR-SDRAM input uses the same LVTTL used with conventional SDRAM. The output and clock use SSTL, which is compatible with high speed data transfer, as the interface. In addition, SSTL compatibility is planned for all input and output in order to realize an even higher level of speed. For conditions such as clock mode and strobe use, which have already been fixed at JEDEC in the pursuit of high speed, standard specifications for the first phase have been established.

Fig. 6 shows the circuit simulation model and simulation results obtained when 8 DDR-SDRAM modules were installed in a system. From the results shown in the figure, it is feasible to design a DDR-SDRAM module with a data transfer rate of 200 MHz based on the design of a conventional SDRAM module.

Hitachi engineers are also studying Rambus for possible use in next-generation high-speed modules. The Rambus memory has a high-speed data transfer rate with the exclusive bus, called Rambus channel, and the synchronized protocol. From a performance point of view, it is expected to attain a 400-MHz clock signal and an 800-MHz data rate for a total data transfer rate of 1.6 Gbyte/s. In order to realize this overall performance, the PCB must be designed for a higher level of performance.

CONCLUSIONS

The development of memory modules at Hitachi, Ltd. and future trends are discussed here. High expectations are held for SDRAM development as high speed memory for use in main memory. However, the history of marketed SDRAM products is still short and the following tasks must be tackled in order to bring the product into widespread long-term use among system users. (1) Lower power consumption is required for application to portable equipment. (2) Pursuit of high speed through intensive investigations into clock modes and strobe use. (3) Establishment of module board design technology capable of high transfer rates of 200 MHz and higher. (4) Improvement in simulation model precision and simulation forecasting technology.

Investigation of these details is required in order to realize high speed and high performance in memory modules. In the future, Hitachi, Ltd., intends to advance development of module products while improving technology. In order to extract and use the maximum memory performance, it is important to target total solutions that strengthen cooperation between memory module designers and system designers and create a common recognition relative to performance improvement.

REFERENCES

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