# Large-Capacity Flash Memories and Their Application to Flash Cards

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*OVERVIEW: Flash cards using flash memory are expected to be the leading removable memory for the various mobile devices that support the next generation of multimedia. A substantial market has been created since the cards started to be used as the storage media for digital cameras in 1997. Also, a large number of types of small flash cards have been proposed and progress has been made on their standardization. Hitachi, Ltd. has used its own AND-type technology to mass-produce 64-Mbit flash memory chips suitable for large-capacity mass-storage applications. These chips are used to produce personal computer advanced technology Aattachment (PC-ATA) interface cards, which have excellent compatibility with many kinds of electronic equipment, and also CompactFlash™* cards. Hitachi makes application specific IC (ASIC) with SuperH and H8 series microcomputer cores as controllers for AND-type flash memory, enabling it to create high-performance flash cards. For the future, Hitachi has started to use multi level cell technology to produce 256-Mbit flash memory chips, and it plans to make high-capacity flash cards of up to 640 Mbytes in the PC-ATA format and 192 Mbytes in the CompactFlash format. Thus it will be possible to use flash memory as a replacement even in systems formerly built with hard disk drives.*

## INTRODUCTION

WE expect flash memory to open up a new market focused on the present rapidly growing mobile information device market even though flash is a different category than conventional memory devices such as dynamic random access memory (DRAM), read-only memory (ROM), and hard disk drives (HDD). In this paper we will discuss the characteristics of the HN29W6411 64-Mbit flash memory optimized for mass-storage applications and the characteristics and applications of memory cards using this chip. We will also discuss the 256-Mbit multi level flash memory for which Hitachi has high hopes as the next-generation flash memory.

## POSITION OF THE AND-TYPE AMONG THE VARIOUS FLASH MEMORY TYPES

Fourteen years have passed since the first announcement of flash memories in 1984. During this time research and development have been energetically carried out on cell technology, circuit technology, and

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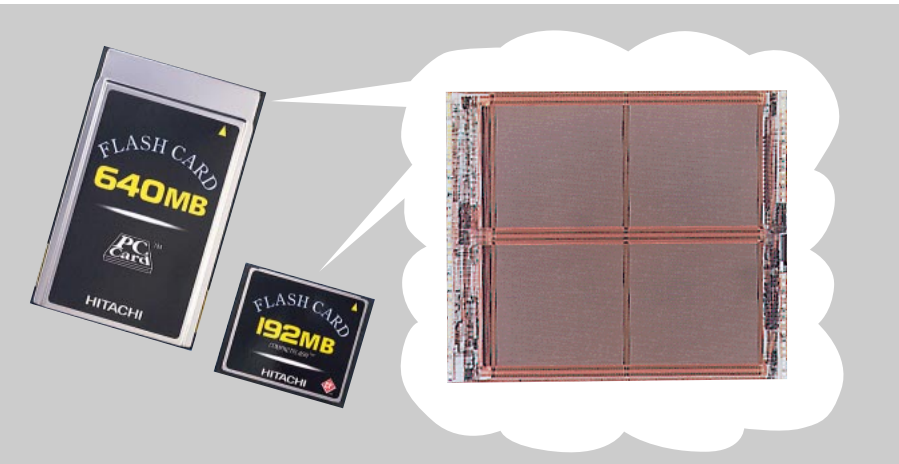



*Fig. 1—256-Mbit Flash Memory Chip and Flash Cards Using These Chips.*
*This photo shows a 256-Mbit flash memory chip that stores 2 bits in one cell using multivalue flash memory technology and flash cards using these chips: a 192-Mbyte Compact Flash Card and a 640-Mbyte PC-ATA card.*

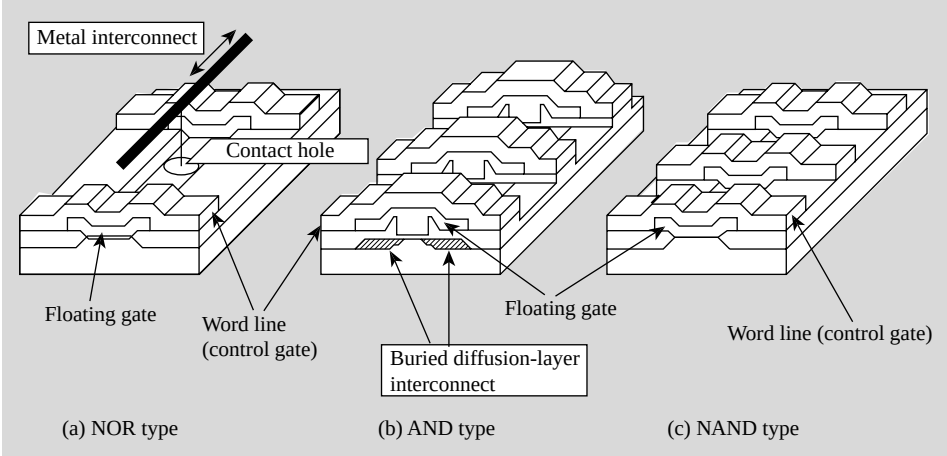



*Fig. 2—AND-Type Memory Device Structure.*
*As shown, sub-data and sub-word lines are fabricated in a buried diffusion layer to produce a contactless structure.*

process technology with the aim of achieving high-density flash memory that operates at low voltage. Including the AND-type developed by Hitachi, flash memory types in production include NOR-type, NAND-type, and DINOR-type products.

AND-type flash memory can be characterized by the following features: data lines and source lines are connected in a parallel hierarchy; in the write state the side with the lower threshold voltage is used; and write and erase operations utilize Fowler-Nordheim (FN) tunnelling. The characteristics of these technologies enable fast readout when operated at a low power supply voltage of 3.3 V. They also enable a small rewrite unit size (write and erase units are the same size) together with high integration density — both of which are important for use in mass storage. Fig. 2 shows the structure of the AND-type memory cell device, while Fig. 3 shows the AND-type memory array circuit. An AND unit consists of m unit cells connected in parallel between a sub-data line and a sub-source line, with two selection transistors connecting the sub lines and the main lines. This memory array has 3 significant features: parallel connection of memory cells, hierarchical arrangement of data lines and source lines, and pseudo contactless structure of the sub lines formed in the diffusion layer.

Because the memory cells are connected in parallel, the necessary current of more than 20-µA for high-speed random readout is available in the same manner as the conventional NOR-type cell. The hierarchical connection arrangement supports higher speed and lower power consumption because the drain-side selection transistor isolates the nonselected AND units from the main data line resulting in a highly significant reduction in data-line capacitance. Moreover, operation of the source-side selection transistor isolates

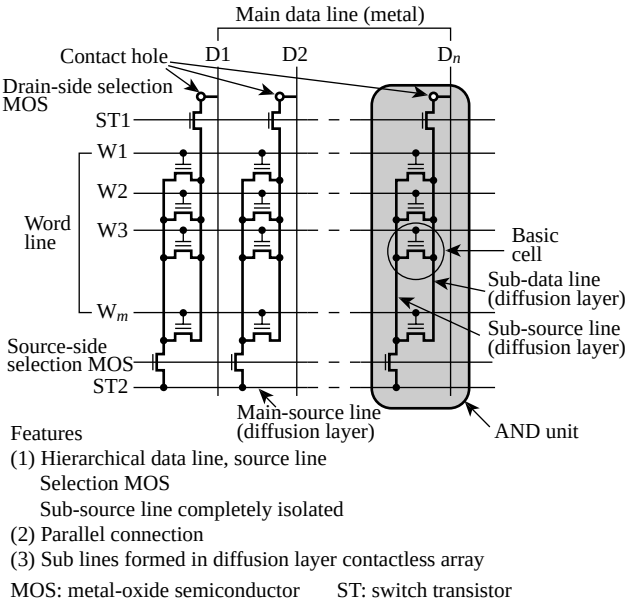



*Fig. 3—AND-Type Memory Array Circuit.*
*The memory array circuit consists of m basic cells connected in parallel between a sub-data line and a sub-source line, and two selection transistors — each of which is connected between one of the sublines and the corresponding main line.*

the sub-source lines from the main-source line, thereby reducing capacitance. Thus a 1:1 relationship between the selected AND unit and the data line can be established. Noise immunity is high, and it has become possible to make the small units of about 512 bits for write and erase coincide perfectly.

## FEATURES OF HITACHI'S FLASH MEMORY

Hitachi used AND cells to develop the 'HN29W6411' 64-Mbit and 'HN29W8411' 84-Mbit flash memory chips suitable for mass storage applications. The most important attribute of mass-storage memories is cost. One technology for solving

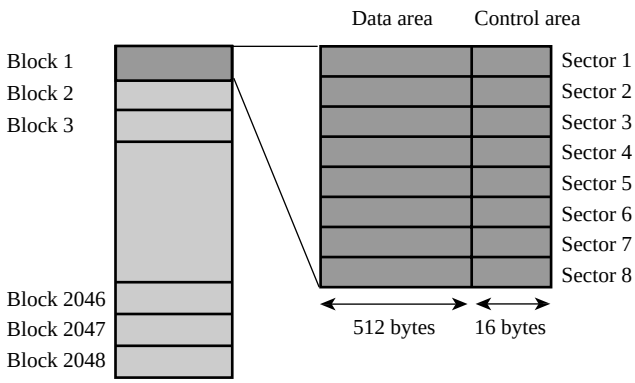



*Fig. 4—Memory Array Configuration.*
*One sector consists of a 512-byte data area and a 16-byte control area.*

the cost problem is use of the AND memory cell, another is use of mostly good memory (MGM) technology.

The usual types of memory use redundant circuits to achieve products that are 100% good with nondefective bits. However, if memories with defective bits can be sold commercially as products, we can expect a reduction in cost. The solution is MGM technology. As shown in Fig. 4, the HN26W6411 memory array configuration consists of multiple sectors each with a 512-byte data area and a 16-Byte control area.

Information on whether there is a defective bit in a data byte is indicated in the control byte enabling the microcomputer that controls the memory to detect the defective sector. Specifications for the HN29W6411 call for more than 98% of the 16,384 sectors to have all-good bits. The principal characteristics of the HN29W6411 and HN29W8411 are shown in Table 1.

## FLASH CARD MARKET

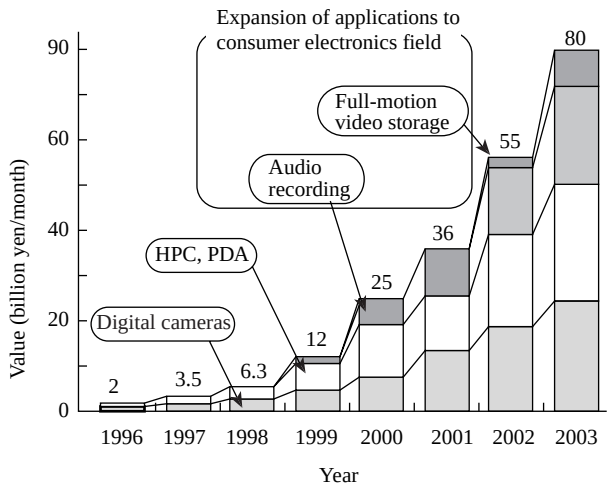
Fig. 5 shows a forecast of demand for flash cards using flash memory. In 1997 sales started for many types of digital cameras using flash cards as the memory media, driving the start of large-scale use of flash cards in the consumer and personal information equipment field. Initially cameras were made mainly for display at video graphics array (VGA) resolution and a 2-Mbyte card was bundled with each camera. Mega pixel high-resolution cameras have since emerged, and now it is becoming common for 8-Mbyte cards to be included.

In the personal computer world handheld computers emerged in which it is hard to install a HDD, and user data and software that was formerly saved in an HDD or battery backed-up DRAM is now stored in cards. In the future we believe that card applications will rapidly increase, including storage of voice and music and also full-motion video.

The most standardized flash card is the PC card compliant with the standards jointly specified by the Personal Computer Memory Card International Association (PCMCIA) and the Japan Electronic Industry Development Association (JEIDA). Recently, mobile devices have become smaller and smaller, and

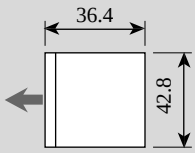
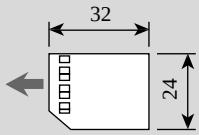
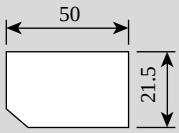
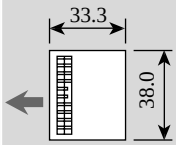
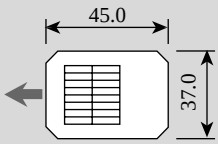
TABLE 1. Principal Characteristics of 64-Mbit and 84-Mbit Flash Memory
*Write, erase, and readout are executed in one sector at a time, and configuration is optimized for file data transfer.*

| Characteristic \ Memory type | | HN29W6411 | HN29W8411 |
|---|---|---|---|
| Power supply voltage | | 5 V±10%<br>3 V±0.3V | 5 V±10%<br>3 V±0.3V |
| Word configuration | | (512+16 byte) × more than 16,057 | (512+16 byte) × more than 21,074 |
| Writing | Speed | 1 ms | 0.3 ms |
| | Unit | 512 byte | 512 byte |
| Erase | Speed | 1 ms | 1 ms |
| | Unit | 512 byte | 512 byte |
| Readout | 1st time | 5 µs | 6 µs |
| | 2nd and above | 50 ns | 50 ns |
| Power consumption | Standby | 5 µA | 5 µA |
| | Operating | 40 mA<br>(3.3-V writing mode) | 40 mA<br>(3.3-V writing mode) |




HPC: handheld personal computer
PDA: personal digital assistants

*Fig. 5—Flash Card Demand Forecast.*
*The flash card market will start up for products such as digital cameras and handheld personal computers, with the market expanding in the future driven by audio recording and full-motion video storage.*

| 100 Comparison characteristic \ Card type | CompactFlash | Multimedia card | Memory stick | Miniature card | Smart media |
|---|---|---|---|---|---|
| External form and dimensions (mm) |   3.3 mm thick |   1.4 mm thick |   2.8 mm thick |   3.5 mm thick |   0.82 mm thick |
| Specifications and I/F | 50-pin PC-ATA, IDE | 7-pin multimedia card spi I/F | 10-pin proprietary I/F | 60-pin flash | 22-pin NAND flash |
| Card components | Embedded high-performance controller | Embedded high-performance controller | Embedded controller | Flash memory only | Flash memory only |
| Maximum capacity | No limit (to the extent that chips can be assembled on printed circuit board) | Depends on capacity of flash memory chips | ——— | Depends on capacity of flash memory chips | Depends on capacity of flash memory chips |

I/F: interface PC-ATA: personal computer advanced technology attachment
IDE: integrated Drive Electronics

TABLE 2. Comparison of Small-Outline Flash Cards
*Mobile devices are becoming smaller and smaller; thus many cards smaller than the PC card have been proposed.*

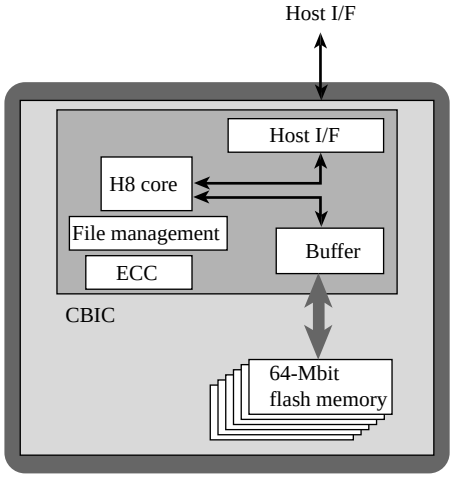
various types of cards even smaller than the PC card have been proposed and adopted, as shown in Table 2. Hitachi has positioned flash cards as a removable media for transfer among multimedia devices and adopted for production of the CompactFlash card because of its excellent compatibility with numerous types of equipment.

## FEATURES OF HITACHI FLASH CARDS

Cards being produced by Hitachi are the PC-ATA card compliant with the PC card specifications that features excellent compatibility, and the CompactFlash card. Both types of cards are recognized by the system as an input/output (I/O) device — as a disk similar to an HDD; therefore a controller is incorporated in the card to provide the functions necessary for file management. A block diagram of the CompactFlash configuration is shown in Fig. 6.

The tasks performed by the controller in order to use AND-type flash memory and make it operate as a file include host interface (I/F) - PC card I/F and IDE I/F, ECC, MGM control of flash memory, and wear leveling.

Because the controller must execute the host I/F procedures and the controller's internal processing in an asynchronous manner, the host I/F bus and the flash memory I/F bus are completely separate structures. Wear leveling is necessary because the flash memory endurance is approximately 10 to the fifth-power ($10^5$) cycles. Thus sectors in the file allocation table (FAT), directory, and other regions that have been rewritten a large number of times are automatically exchanged with sectors that have been rewritten fewer times to level the number of endurance cycles across the memory. This action effectively lengthens the life of the memory, and is a necessary function for file storage.




ECC: error corection code CBIC: cell-based IC

*Fig. 6—Compact Flash Block Diagram.*
*Complex control functions are implemented in the CBIC.*

The flash card product family presently available is shown in Fig. 7. Market requirements for flash cards include higher capacity, higher performance, and especially higher writing speed.

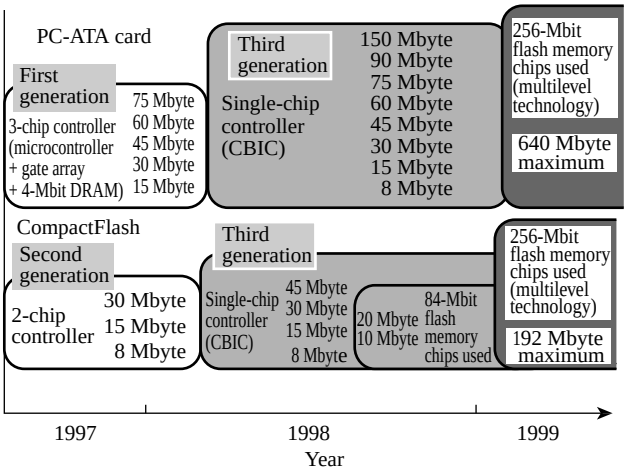



*Fig. 7—Hitachi's Flash Card Product Family. Currently implemented cards include PC-ATA cards to 150-Mbyte and CompactFlash cards to 45 Mbyte.*

With regard to higher capacity, megapixel cameras featuring one-million or more pixels have emerged among the digital cameras that are today's main application, and the memory capacity required for a single picture has surged up to a large 700 kbyte – 1 Mbyte. Thus the cards bundled with cameras are 8 Mbyte, and 32 – 45-Mbyte cards are the most widespread among options. Use of high-capacity flash memory chips and the multilayer TCP technology that enables high-density packaging has made it possible to provide a product selection appropriate for the market.

At present 64-Mbit flash memory chips are used in PC-ATA cards with capacities up to 150 Mbyte and CompactFlash cards with capacities up to 45 Mbytes. In the future, 256-Mbit chips now being developed will be used in PC-ATA cards with capacities up to 640 Mbytes and CompactFlash cards with capacities up to 192 Mbytes. Upcoming 256-Mbit chips will be discussed in the following section.

Fig. 8 shows a cross-section view of a 45-Mbyte CompactFlash card. As there are only three locations on the PCB on which flash memories can be assembled, two types of TCP chips with short and long leads are stacked in two layers at each location. Thus a maximum of six flash memories can be assembled and a total capacity of 45 Mbytes can be realized.

Writing performance is the most difficult characteristic of presently available flash memories, and innovations for its improvement are an important aspect of controller design. In 3rd-generation flash cards that use 2 or more memory chips with a total capacity of more than 15 Mbytes, the controller writes

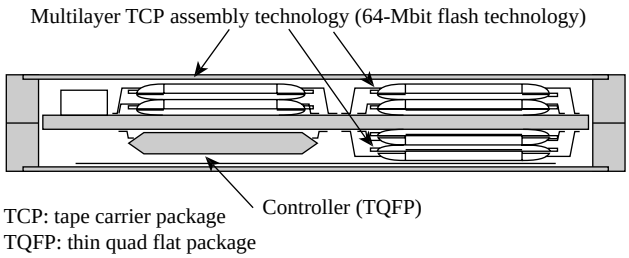



*Fig. 8—Cross-Section of 45-Mbyte CompactFlash. Flash Multilayer TCP Assembly Enables Realization of 45-Mbyte Configuration.*

the data to two flash memory chips simultaneously by using two internal buffer memory. Thus writing performance is improved to 350 kbit/s from the 250 kbit/s for 8-Mbyte cards. Moreover in 4th-generation flash cards, high-speed flash memory (64 Mbit A mask or 84 Mbit) chips are used, and speeds of 500 kbit/s can be realized even for 8-Mbyte cards.

## FUTURE DEVELOPMENT

The trump card expected to reduce the cost of flash memory is multilevel cell technology. Hitachi has developed 2-bit multilevel memory cell technology to store 2 bits of information in a single cell. It has used this technology to develop the world's first flash memory product of this type. With this technology, smaller chip sizes can be realized for 256-Mbit flash memories fabricated with 0.25-µm technology than 64-Mbit flash memory fabricated with 0.35-µm technology.

If this 256-Mbit flash memory is used, implemen-

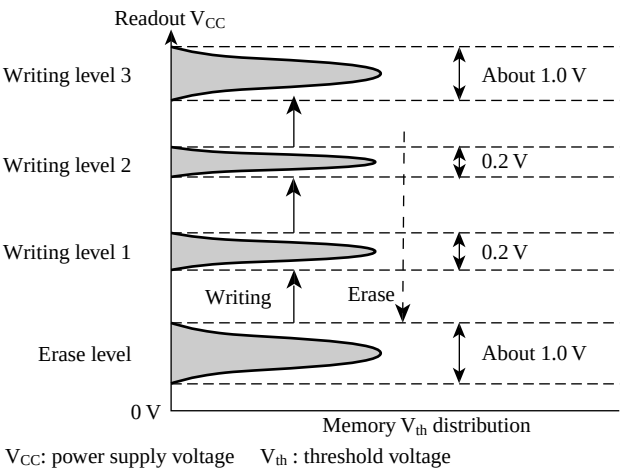



*Fig. 9—Threshold Distribution of Multilevel Memory. Multilevel flash memory cell threshold voltage must be matched within the narrow range of ± 0.1 V in a short period of time.*

tation of PC-ATA cards with a capacity of 640 Mbytes and CompactFlash cards with a capacity of 192 Mbytes is not only technologically but also economically feasible. Thus the range of applications should broaden to include replacement of small HDD drives used for backup in routers and other types of communications related equipment. Features and performance of 256-Mbit flash memory will be discussed below.

### Enhancement of Writing Performance

Multilevel flash memory cell threshold voltage must be matched within the narrow range of ± 0.1 V, as shown in Fig. 9, in a short period of time. To match threshold voltage in a short period of time, it is necessary to reduce the variation in write time among memory cells. The variation in writing speed for 256-Mbit flash memory was reduced to less than 10× by improvements in process technology.

Write processing time was also reduced by an on-chip processor optimized exclusively for write processing that controls such conditions as applied programming voltage and verification timing. Thus we were able to realize a write time of only 1 ms per sector, the basic writing unit. Moreover, by making the largest writing unit 2,112 bytes — 2,048 data bytes + 64 control bytes, which is 4× that of the 64-Mbit flash memory, a maximum write performance of 2 Mbit/s is realized.

### Readout Speed

After receiving a read command, there is a waiting period of 50 µs, and then individual bytes up to a maximum of 2048 are transferred serially from the I/O terminal at a rate of 50 ns/byte.

### Reliability

It is often necessary to implement error checking and correction code (ECC) when using flash memory to maintain system reliability. Normally, ECC is either incorporated in the host as hardware or implemented as so ftware processing. In the 256-Mbit flash memory, we are considering adding on-chip processing to decrease the load on the host.

### MGM

The 256-Mbit flash memory is comprised of a total of 16,384 sectors in the same manner as current 64-Mbit flash memories. However each sector consists of 2,112 bytes. They are supplied to the market as MGM devices with good sectors amounting to more than 98% of the total.

## CONCLUSIONS

In this paper we have discussed large-capacity flash memories and their application to flash cards. Cards using high-capacity flash memories feature low power consumption, small size, thin profile, and high reliability making them ideal for such products as digital cameras and mobile information devices. We also think that a wide range of storage applications for industrial equipment will evolve. Hitachi will devote considerable resources into developing large-capacity flash memory technology and products with the aim of promoting an greatly enlarged market for flash memory in mass-storage applications.

## ABOUT THE AUTHORS

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