System ASIC Technologies for Mounting Large Memory and Microcomputers

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OVERVIEW: Mobile information devices and all other multimedia devices are currently enjoying an active market. It is not sufficient to concentrate multiple functions within these devices; they must be small, light, and low power-consumption systems. Hitachi, Ltd.'s response to these requirements is to propose system application specific ICs (system ASIC). The 0.8-µm process HG71C series micro cell based IC (µCBIC) with on-chip central processing unit (CPU) evolved into the 0.5-µm process HG72C series and then the 0.35-µm process system ASIC series. The 0.35-µm system ASICs in mass production are the HG73C series µCBIC with on-chip CPU and the dynamic random access memory (DRAM) merged HG73M series that in addition to a CPU can have on-chip DRAM. The on-chip DRAM eliminates the memory bus bottleneck enabling realization of high performance. Now, Hitachi is in the midst of migrating its 0.35-µm system ASICs to a finer-pattern 0.18-µm process. Already the forerunning cell-based HG75C series is in production. The HG75C series uses a 0.18-µm complementary metal-oxide semiconductor (CMOS) process technology with 5 layers of metal interconnect that enables 5 times the integration compared with the HG73C series, less than 1/5 the power consumption, and 2 – 3 times higher-speed operation — which has expanded the range of solutions immensely (Fig. 1). In the near future Hitachi proposes to include the SuperH core, analog modules, and other IP modules. Furthermore, for graphics related applications DRAM-ASICs will be fabricated with the aim of providing full-fledged system ASICs.

Fig. 1—Finer Pattern Processing of Hitachi System ASICs Steadily Progresses.
Hitachi system ASICs are in the midst of migrating from a 0.35-µm process to a 0.18-µm process. Use of a 0.18-µm process compared with a 0.35-µm process enables a 5-times increase in integration level, reduction in power consumption to less than 1/5, and a 2 – 3 times increase in speed.
INTRODUCTION
DURING the past 1 or 2 years mobile information devices have made remarkable progress in extending their use among the general population; so much so that they can be considered to be an indispensable lifestyle item. The advancing wave of full-motion video for multimedia now extends to the mobile category. Not only mobile information devices but all multimedia systems store huge quantities of data, and require high-speed processing. At the same time mobile devices are required to reduce system size and weight. Also required is incorporation of versatile high functionality. Hitachi has responded to these requirements by offering system ASICs. Already in 0.35-µm system ASICs it is producing in volume the HG73C series micro-cell based ICs (µCBIC) with central processing unit (CPU) cores: the 32-bit reduced instruction set computer (RISC) SH-1 and SH-3 microcomputers and the 16-bit H8S microcomputer.

Also in production is the DRAM merged HG73M series that has the same 150-MHz high-performance logic as the HG73C series and makes possible the addition of on-chip DRAM with the CPU. Now the door to the system on chip has been opened with the further progress to the even finer 0.18-µm process HG75C series system ASIC, as shown in Fig. 2. In this paper we will discuss the features of Hitachi’s system ASICs that have progressed toward finer patterns and higher integration, and also future plans.

SYSTEM ASIC LINEUP
The µCBIC family of cell-based ICs with on-chip CPUs together with DRAM merged ASIC are the twin branches of Hitachi’s system ASIC. Among these products the HG73C series, which uses a 0.35-µm process, is the mainstay with a practicable scale of 5-million gates on chip — including a CPU and high-speed high-accuracy A-D and D-A converter modules, compiled ROM and RAM, static RAM (SRAM), and user logic. Available CPUs for the HG73C series have the same functionality as Hitachi’s standard 32-bit RISC-type SuperH, SH-3 and SH-1 microcomputers, and also the 16-bit complex instruction set computer-type (CISC) H8S, as shown in Fig. 3. Since SH-1 and H8S make use of compiled cores, peripheral functions can be customized by running the microcomputer compiler tool supplied by Hitachi on a workstation.

For the graphics processing necessary for multimedia, fast logic must be augmented by large-scale memory. The required capacity is virtually impossible to implement in SRAM, which like the ASIC process has planar memory cells with only a
low integration level. For example, in a 0.35-µm ASIC, the maximum possible SRAM capacity is said to be about 1 Mbit.

With the general purpose DRAM that is driving finer patterning of semiconductors, advances are being made in three-dimensional structures and higher densities, leading to the realization of order-of-magnitude larger memory capacities. Thus the DRAM-ASIC that incorporates a large-scale DRAM module is drawing attention as strongest challenger for the leading role in system-on-chip products.

The principal merit of DRAM on chip is elimination of the bus bottleneck. A system board is completely implemented on a single chip so the buses between logic and memory can be expanded enabling high-speed processing. If we do not make allowance for efficiency and we maintain constant clock speed, then bus width directly affects bus performance. If we consider the simplest possible system consisting of standard DRAM and logic with a standard DRAM bus width of 8 bits and a clock frequency of 66 MHz, then transfer performance is a mere 66 Mbyte/s. However on a DRAM-ASIC it is relatively easy to expand the bus width to about 128 bits, and bus transfer performance will exceed 1 Gbyte/s.

The DRAM-ASIC not only makes for improved efficiency by eliminating the bus bottleneck; by implementing memory and logic on the same chip it contributes to smaller system size. Moreover drivers for an external bus become unnecessary thereby reducing power consumption.

Hitachi as a standard DRAM vendor offers a 64-Mbit DRAM. The HG73M series incorporates the same 64-Mbit DRAM technology and also a DRAM-module creation technique called DRAM micromodule architecture that defines a method for achieving DRAM-ASICs that features high performance, low power consumption, and reduced size. This method utilizes 3 types of components to construct DRAM modules: memory array

![Fig. 3—CPU Core Roadmap.](image)

Hitachi µCBIcs with CPUs on chip, which debuted as the HG71C series with the H8/300 on chip, have reached the HG73C series that make possible on chip the same functions as 32-bit RISC type standard microprocessors SuperH (SH-3 and SH-1) and 16-bit CISC type H8S. The 0.18-µm HG75C series will make possible the SuperH on chip.

![Fig. 4—Example of 0.35-µm DRAM-ASIC.](image)

Hitachi’s DRAM-ASIC HG73M series utilizes 3 types of components to construct DRAM modules: 256-kbit memory array micromodules; a shared module for input and output (I/O), and a power supply module. DRAM capacity can be varied within the range of 1 Mbit to 4 Mbit in increments of 256 kbits. Moreover multiple DRAM modules can be arranged on the same chip. Multiple DRAM modules can be implemented on the same chip.
micromodules with a capacity of 256 kbits in multiples of 4 – 16 banks; a shared module for input and output (I/O), and a power supply module. DRAM capacity can be varied within the range of 1 Mbit to 4 Mbit in increments of 256 kbit. Moreover multiple DRAM modules can be arranged on the same chip (Fig. 4).

Because standard DRAMs have a limited number of external pins, many engineers have strained to develop innovative addressing methods, I/O configurations, and bus widths that reduce the number of pins. However, these innovations cause difficulties in applications and degrade performance. The absence of a limitation on internal interconnects that is the most significant advantage of on-chip DRAM is utilized in the HG73M to realize high-performance DRAM modules. The major differences between a standard DRAM and the DRAM modules on the HG73M caused by the allowable number of pins or internal interconnects is shown below.

Memory modules may have about 300 internal interconnects while standard DRAM is limited to about 50 pins. Thus memory modules use completely independently controlled row and column addresses, while standard DRAM uses multiplexed row and column addresses. Input and output in the memory modules are separate while standard DRAMs used shared I/O. Moreover the memory modules use a bus width of 128 bits, while standard DRAMs have bus widths of × 1, × 4, or × 16.

The HG73M series uses a process optimized for embedded DRAM enabling the implementation of 150-MHz high-performance logic equivalent to the HG73C series together with DRAM on chip. Also, the HG73M series can have on chip the SH-3 and SH-1 high-performance 32-bit RISC microcomputers and the H8S 16-bit CISC microcomputer in the same manner as the HG73C series. The design environment used for the HG73M series is the System ASIC Unified Design Environment that it shares with the HG73C series.

Hitachi supplies users with HDL model for the DRAM modules in the same manner as for the CPU modules.

0.18-µm PROCESS USED FOR THE HG75C SERIES

Demands are steadily increasing for smaller, higher speed, and lower power consumption multimedia devices and mobile information devices. Hitachi is responding to these demands by migrating its semiconductor processes toward finer patterning, and it is now producing 0.18-µm process system ASIC as the cell-based IC HG75C series. Technology used in this series is a 0.18-µm CMOS process with 5-layer metal interconnect. Compared with the earlier HG73C series, 5 times the level of integration, less than 1/5 the power consumption, and 2 – 3 times higher speed operation can be achieved. Circuits with a scale of about 25-million gates are estimated in case of on chip designs using only random logic.

When operating with a power supply voltage of 1.8 V, the low power consumption of 0.04 µW/gate × MHz is realized. Gate propagation delay is only 75 ps for a 2-input NAND with a standard load, making it possible to implement a 300 – 400 MHz high-speed system LSI. Both single-port and dual-port synchronous SRAMs are also supported.

HG75C design is carried out using the same system ASIC design environment, an overall design environment using commercial EDA tools on a workstation, optimized for the HG73C series and the HG73M series. To cope with the increase in time required that obstructs design and verification of truly large-scale HG75C series circuits in the 1-million gate class, Hitachi will phase in support of new tools including a cycle-base simulator, static timing analysis tool, and a formal verification tool. This should greatly reduce verification time compared with the present environment that mainly uses an event-driven simulator.

As the first phase of the HG75C series, core cells, I/O cells, and SRAM cells have been released. As the follow-on phase 2, analog cells and SuperH core will be released. Also, for phase 2 we intend to generate internally the V_{BB} control voltage that must now be supplied externally.

IP MODULE LINEUP

With the advent of higher levels of integration and higher functionality, in addition to the CPU cores and large-scale DRAM modules described here, requirements for intellectual property (IP) modules have increased. IP implements functions endorsed by standardization bodies such as the Institute of Electrical and Electronics Engineers (IEEE) or functions that are widely adopted and used by the industry and thus constitute indispensable elements for implementing systems on chip.

Recently the Virtual Socket Interface Alliance (VSI) has promoted overall standardization of IP. By providing IP in the form of an ASICs library to users, the man hours needed to design LSIs can be reduced
and it alleviates the burden on users.

Hitachi is proceeding with the following IP lineup to meet the needs of various application fields.

1. Personal computer peripherals: universal serial bus (USB), IEEE 1284, IEEE 1394, Infrared Data Association (IrDA), peripheral component interconnection (PCI).
2. Graphics: National Television System Committee (NTSC)/phase alternation by line (PAL) encoder.
3. Network systems: controller area network (CAN), Ethernet*, and others.

These forms of IP are usually used with a microcomputer and controlled by it. Thus in the past a microcomputer LSI and — for example — an IEEE 1284 chip and others were assembled on a board as multiple chips to build a system. With Hitachi’s system ASIC, these IP modules and microcomputer CPU cores can of course be implemented on chip; moreover a user logic can also be integrated on the same single chip to implement a system on chip.

As an example of a system ASIC implementation with an IP module on chip, a µCBIC for printer system with an on-chip USB function module, which is a form of serial interface, is shown in Fig. 5.

By using IP modules, even when developing this type of high-functionality ASIC, users need only develop their own user logic, and development of a large-scale ASIC becomes quite simple. In general, most of IP is compliant with various adopted standards specifications. However, within a single IP there may be a section of the circuit configured according to standard specifications and also a section of the circuit that is nonstandard because it is dependent on the user specification or application.

If we take the USB as an example, the UDC core section is uniquely determined by specifications of the USB protocol, but there can be differences in the configuration of the interface core section. For example, for a printer application the number of end point (FIFO) buffers is in principle 3, but according to user specifications there may be 4. Also, for applications other than printers the number of buffers and their capacity can change. Thus Hitachi takes a flexible approach and has available many types of USB function modules with differing numbers of endpoint buffers with different buffer capacity.

As can be seen from the USB example, it is not sufficient to merely have IP modules available in the form of macro blocks. When developing system ASICs, it is extremely important to be able to take a flexible approach with respect to conditions including user specifications, the application, and microcomputer interface. Also, hardware support alone is insufficient, and support including firmware is necessary for microcomputers. Hitachi intends to supply all kinds of required support.

At present Hitachi is mainly promoting IP modules in the HG73C and HG73M product lineup. In the

* Ethernet is a registered trademark of Xerox Corp. of the U.S.
future it will promote IP modules in the HG75C system ASIC, and plans to have an even fuller range of IP including CPU core and analog modules (Fig. 6).

CONCLUSIONS

In this paper we discussed Hitachi’s system ASICs comprised of on-chip CPU µCBICs and DRAM-ASICs that are evolving with finer patterns and higher integration. The HG73C series and the HG73M series using a 0.35-µm process are the main products today. Hitachi has now developed the HG75C series as its first 0.18-µm system ASIC product. Among mobile information devices there is not only increasing demand for smaller size and lower power consumption; additionally in the graphics field there is increased demand to eliminate the bus bottleneck that accompanies the large-scale memory necessary to build high-performance systems. Integration of both high-performance CPU and large-capacity DRAM on a single chip will require even finer process technology. Establishing a high-efficiency system on-chip development environment and providing a complete IP lineup are key points in developing 0.18-µm system ASICs and the follow-on next generation products.

REFERENCES


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