The Outlook for Semiconductor Processes and Manufacturing Technologies in the 0.1-µm Age

OVERVIEW: In the 0.1-µm age, it will be possible to build more than one billion transistors on a silicon chip welcoming in the “system-on-a-chip” era. This age will feature an even greater demand for high-performance and low-cost characteristics in LSIs, as well as Quick Turnaround Time (QTAT) from development to production. Device technologies and process technologies have progressed dramatically in recent years, with advanced technologies being driven not only by Dynamic Random Access Memory (DRAM) but also by logic products like microprocessors. Specifically, DRAM has been driving memory cell technologies and fine-processing technologies, and logic products have been driving high-performance transistor technologies and multilevel wiring technologies. Issues in the fabrication of memory cells are the selection of capacitor structure and its insulator film. On the other hand, the major issue in fine-processing technologies is dealing with inherent limits to miniaturization with excimer laser exposure equipment, and for feature sizes of 0.1 µm and smaller, shorter wavelengths or electron beam drawing will have to be selected. Achieving multilevel wiring technologies, moreover, will require the construction of a high-speed wiring system by decreasing wire resistance and decreasing inter-wire capacitance. In production technologies, innovative schemes for raising productivity will be needed to lower costs and deal with shorter product life cycles. Devising QTAT and high-yield technologies to shorten the time from development to production is an important issue here.

RISC: reduced instruction set computer
F-ZTAT: flexible zero turnaround time
SGI: shallow groove isolation
CMP: chemical-mechanical polish
IMO: inter-metal oxide
SOI: silicon on insulator

Fig. 1—Increase in RISC Performance Due to Miniaturization and Application of Advanced Processing Technologies. Hitachi, Ltd. has been raising the performance of system LSIs through the development of fine-processing technologies and multilevel wiring technologies. The SuperH series of RISC processors are becoming faster and consuming less power over time.
INTRODUCTION
In response to the 1994 publication of the “Technology Roadmap for Semiconductors” by the Semiconductor Industry Association (SIA) in the United States, the semiconductor industry around the world has been accelerating its development efforts to achieve the proposed targets early. Since 1997, however, the SIA Roadmap has been revised yearly, and its most recent version will have moved up the 0.1-µm (gate length in logic devices) age by two years (Fig. 2). With regard to manufacturing technologies, major factors behind this revision have been flattening of the process surface by the introduction of Chemical-Mechanical Polish (CMP), and further progress in fine-processing technologies through the application of excimer laser exposure equipment and resolution enhanced technology. It is also considered that miniaturization has been accelerating due to competition in producing low-cost Dynamic Random Access Memory (DRAM) and the achievement of higher speeds and lower power consumption in LSIs targeted for system-on-a-chip applications.

This paper will focus on the 0.1-µm age due to arrive in 2001. We will describe high-performance-oriented device technologies and associated process technologies for shortening development Turnaround Time (TAT) and achieving high yields, all from the viewpoint of lowering cost in terms of production technology.

DEVICE TECHNOLOGIES
High-performance Transistors
Developing high-speed and low-power-consuming LSIs is essential to achieving a system-on-a-chip configuration. In particular, high-speed operation is necessary to perform complex and advanced information processing, and low power consumption is indispensable to achieving long operation time in portable equipment and decreasing dissipated heat in large-scale systems.

To achieve high-speed operation, high-speed characteristics have been sought in Metal-Oxide Semiconductor (MOS) transistors, the basic devices of LSIs. In this regard, a critical factor in achieving high-speed performance is gate delay time in the transistor. The change in gate delay from one generation to the next is shown in Fig. 3. As can be seen, operation speed has been increasing every generation as drive voltage decreases. An important point here is that current can be made large even if drive voltage drops by shrinking the gate length and by making the gate insulator film thinner. However, as tunnel current increases for gate insulator film under 2 nm in the case of SiO₂, studies have begun on...
applying high-dielectric-constant materials like TiO$_2$ and Ta$_2$O$_5$.

In addition to increasing transistor speed, it is also necessary to reduce various parasitic effects to achieve high-speed LSIs. To this end, studies are being made on introducing metal electrodes to lower the resistance of gate electrodes and on applying a Silicon on Insulator (SOI) substrate to reduce parasitic capacitance.

To reduce power consumption, work proceeds on reducing voltage (Fig. 3). In the 0.1-µm age, drive voltage will have to be reduced to 1.2V.

**DRAM Memory Cell**

Systems with built-in DRAM are receiving particular attention in system-on-a-chip development. Incorporating large-capacity memory requires shrinking of memory cell dimensions and integration with the logic process.

A DRAM memory cell basically consists of one transistor and one capacitor. Here, the resistance of word and bit lines increases due to miniaturization, presenting an obstacle to high-speed operation. Therefore, to reduce resistance, the plan is to adopt metal wiring such as tungsten. Furthermore, to store signal charge having a sufficient noise margin, it will be necessary to achieve a nearly fixed value of capacitor capacitance in the memory cell area that becomes smaller every generation. For this reason, surface area of the capacitor is being increased and high-dielectric-constant film is being introduced.

To achieve stable operation in memory cells, charge storage time (refresh time) must be lengthened. As dimensions decrease, the storage-node junction field will naturally become larger, which will in turn increase junction leak current and shorten refresh time. These problems can be solved by preventing the junction field from becoming larger by some means and by increasing capacitor capacitance.

**PROCESS TECHNOLOGIES**

**Fine-processing Technologies**

Fine-processing technologies were originally driven by the large-scale integration of DRAM. Considering, however, that the gate length in logic systems are shrinking rapidly to feature sizes of 0.2 µm and smaller, fine-processing technologies are coming to be driven by both DRAM and logic systems.

The trend toward miniaturization in lithography technology is shown in Fig. 4. Traditionally, smaller feature size has been achieved by shortening the wavelength of the light source. For the 0.1-µm age, a KrF (wavelength: 248 nm) or ArF (wavelength: 193 nm) excimer laser will be used as a light source. In addition, the phase-shift method and resolution enhanced technology (deformed illumination) will be applied to resolve dimensions under the wavelength. Here, application of the phase-shift method will require development of Optical Proximity Correction (OPC) technology, mask-manufacturing technology by high-precision electron beam (EB) drawing equipment, high numerical aperture (NA) exposure equipment, and high-resolution resists.

In dry-etching technology, there will be a need for fabricating high-aspect-ratio structures as feature size decreases. In particular, the fabrication of gate electrodes will require high-precision control of dimensions and shapes and high selectivity with respect to underlying insulator films. Moreover, as the thickness of gate insulator films will become thinner to 2 nm and less, it is essential that etching technology be developed that does not cause charge-up and other kinds of damage.

**Wiring Technologies**

Wiring technologies have been driven by multilevel wiring in logic devices. Here, the flattening of inter-layer insulation film by the introduction of SiO$_2$-film CMP technology for feature sizes of 0.3 µm and less...
Fig. 5—Cross Section of 0.1-µm CMOS LSI Multilevel Wiring Structure.

Flat wiring is achieved through simultaneous copper-based embedding of wires and via-holes (dual damascene method). To connect with the Si substrate, however, tungsten is embedded to prevent the copper from becoming contaminated. Moreover, to support a high-speed wiring system, low-dielectric-constant film is used for inter-layer insulation.

Fig. 4—Trend in Minimum Feature Size and Corresponding Resolution Limit in Lithography Technology.

Miniaturization of logic devices is accelerating compared to that of DRAM. The 0.1-µm age will be supported by applying resolution enhanced technology to KrF and ArF excimer-laser exposure equipment. For smaller feature sizes, it will be necessary to select either shorter wavelengths for exposure or EB drawing.

has accelerated miniaturization. At 0.2 µm and less, the use of CMP technology is being expanded to the formation of tungsten plugs in via-holes and to the flattening of metal systems such as embedded wiring formations made of copper.

A cross section of the basic structure behind 0.1-µm Complementary MOS (CMOS) multilevel wiring is shown in Fig. 5. To solve the problem of Resistance-Capacitance (RC) delay here that accompanies miniaturization, copper will be used as wiring material considering its low resistance at half that of aluminum, the material used up to now. In addition, a low-dielectric-constant film like Spin on Glass (SOG), whose dielectric constant is even lower than that of SiO2, will be used as inter-level insulation film. Application of CMP technology will promote the adoption of a fabrication system that simultaneously embeds via-holes and wiring using copper (dual damascene method).

In the wiring process of the dual damascene method, a two-step structure must be formed consisting of a via-hole and a wiring groove, and this requires highly selective dry etching for different insulator films. High-aspect-ratio structures, on the other hand, will require the development of plating technologies to form barrier metals (to prevent diffusion of copper into inter-level insulation films) and to embed copper, and film-formation technologies to form associated seed layers, etc.
**DRAM Capacitor Technologies**

The most important factors affecting the DRAM process are capacitor structure and selection of its insulator films. At Hitachi, DRAM development has centered about a stack-type memory cell. The changes undergone by capacitor insulator films in DRAM from one generation to the next are shown in Fig. 6. In a stack memory cell, the height of the lower capacitor electrode must be no greater than 1 \( \mu m \) or so considering ease of formation. Accordingly, a tantalum pentoxide (Ta\(_2\)O\(_5\)) film was adopted at the 256-Mbit level instead of the conventional SiO\(_2\)/Si\(_3\)N\(_4\) composite film for the capacitor insulator film. From the 1-Gbit level, a Metal-Insulator-Metal (MIM) structure will be adopted in place of the conventional Metal-Insulator-Silicon (MIS) structure. For the insulator film at this level, the use of Ta\(_2\)O\(_5\) or the introduction of barium strontium titanate (BST) having an even higher dielectric constant is being studied.

An MIM capacitor features a major change in that metal is used for the lower electrode. This metal must have high anti-oxidation properties, and ruthenium and platinum are now being studied as candidates. In addition, barrier materials must be developed to ensure conductivity with underlying Si.

**PRODUCTION TECHNOLOGIES**

**Shortening Development TAT**

As the miniaturization in semiconductor technology accelerates and the shift toward system-on-a-chip devices progresses, a wide variety of LSI products will need to be developed in short periods. Their production time will need to be shortened as well. Shortening of TAT in LSI development and launching production in a short time will therefore become major issues.

In the prototyping stage, TAT must be shortened. To this end, a Super Quick TAT (SQTAT) line can be constructed by increasing the application ratio of single wafer processing equipment. Process monitoring and early detection of defects by developing inline measurement and analysis technology will also be necessary. Defect detection must include those of minute proportions, which means that defect inspection and classification will need to be performed by Scanning Electron Microscope (SEM) means in addition to inspection by conventional optical means.

Technology for analyzing defects in prototyped LSIs is important in shortening development TAT. Here, to locate defect position, a variety of methods will have to be developed, including detection of defect-related optical and thermal generation in LSIs, detection of changes in picture contrast using SEM equipment and the like, direct measurement of transistors, resistors, and other devices by nanoprobes, and estimation of defect position by circuit Design Automation (DA).

**High-yield Technology**

To lower costs in the face of shorter product life cycles, it will be necessary to achieve high yield in a short time period at the production stage. It therefore becomes important to incorporate yield considerations at the LSI design and process development stages.

In the design stage, circuit design will be performed based on performance prediction that takes dispersion in transistor characteristics and other factors into account. Layout design, moreover, will make use of Critical Area Analysis (CAA) that performs prior evaluation on how the number of particles and pattern defects might affect yield. While it is known that the manner in which the number and size of particles affect yield differs according to the layout method, determining that sensitivity in quantitative terms is a subject for study.
In process development, dispersion in transistor characteristics, resistance, capacitance, etc., will be evaluated beforehand by prototyping a Test Element Group (TEG), and the results of this evaluation will be reflected in circuit design. In addition, each process technology will incorporate quality-engineering techniques to establish stable process conditions. It will also be necessary to raise the sensitivity and accuracy and expand the applicability of conventional quality control (QC) technologies associated with dimensions and film thickness, impurities, breakdown voltage of insulator films, resistance, etc.

CONCLUSIONS

This paper has described semiconductor device technologies, process technologies, and production technologies for the 0.1-µm age that will help welcome the system-on-a-chip era.

This device age will demand even higher levels of LSI performance and lower costs as well as QTA T from development to production. Due to lack of space, we have focused here on those technologies especially appropriate to meet these demands. There are still many outstanding issues and various technologies will have to be developed to solve them. Overcoming these problems in a steady manner will contribute to the future expansion of the semiconductor industry.

REFERENCES


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