Semiconductor Device Manufacturing & Inspection Equipment

1 Cutting-edge Semiconductor Device Technology Trends and Diversifying Customer Needs

The demand for semiconductors is growing as a core technology for supporting a digital society utilizing the Internet of Things (IoT), artificial intelligence (AI), fifth generation (5G) mobile network communication, and autonomous driving, etc. Moreover, semiconductors are an important strategic technology for which many countries are deploying large-scale industrial policies from the perspective of economic security.

Further miniaturization of cutting-edge semiconductor devices is proceeding with the implementation of extreme ultraviolet (EUV)*1 lithography. In terms of advanced logic, more complicated transistor structures and chip-level integration techniques are being introduced. Moreover, an increase in the number of layers in 3D-NAND flash memory and the dimensional scaling and three-dimensional (3D) structure of dynamic random access memory (DRAM)*2 are required to improve the memory storage density.

Sub-nanometer-order processing accuracy and the metrology and inspection accuracy to control that processing are required in manufacturing, metrology, and inspection systems for such cutting-edge semiconductor devices. Moreover, stricter controls are required for the management of defects and variations caused by EUV lithography and the particles that occur during processing by each manufacturing system. To shorten the development time and improve the yield, the demand for high-precision analysis to identify device fault locations is also increasing.

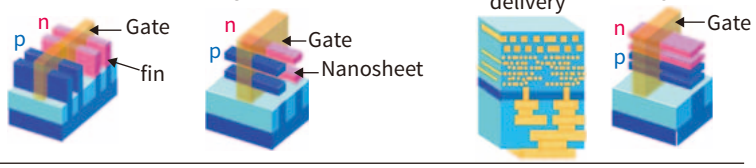
The Hitachi Group is committed to providing solutions for diversifying customer needs.

(Hitachi High-Tech Corporation)

*1 Extreme ultraviolet light source with a wavelength of 13.5 nm.
*2 Memory element that stores electric charge in a capacitor to retain information.

Cutting-edge logic device

Year	2021	2022	2023	2024	2025	2027	2030
Technology node (nm)	7–5	5–3		3–1.8		1.5	1.0
Gate pitch (nm)	51	48		45		42	40
Metal pitch (nm)	30	24		20		18	16
Transistor structure	Fin FET		GAA		Backside power delivery		3D



Memory device

Year	2021	2022	2023	2024	2025	2027	2030
DRAM technology node (nm)	15		13	12–11	10		3D
Number of 3D-NAND layers	128	–176		200–400	400–600		600–

Estimated by Hitachi High-Tech based on the International Roadmap for Devices and Systems 2022 and other sources.

Fin-FET: fin field-effect transistor GAA: gate-all-around, a field-effect transistor with channel sidewall surrounded by gates on all sides

1 Progress in cutting-edge semiconductor devices

2 Electron beam area inspection system GS1000

2 Electron Beam Area Inspection System GS1000 Responds to Growing Inspection and Metrology Needs with EUV Lithography

Cutting-edge device manufacturers providing advanced server/mobile processors to the market are increasing the application of EUV lithography processes in the high-volume manufacturing (HVM) of 5-nm generation devices and the research and development (R&D) of 3-nm generation devices. Miniature and high-precision patterning processing is possible with an EUV lithography technique, but the metrology of EUV-specific pattern width variations and the inspection of randomly occurring minute stochastic defects[*1] are required. In addition, the needs for high throughput inspection and metrology are increasing to realize high-quality EUV mask transfer processes.

Hitachi High-Tech Corporation developed the electron beam area inspection system, GS1000, which supports high-speed, high-sensitivity, and wide-area scanning to help solve such issues in processes that apply EUV lithography processing. This product achieves wide-area imaging through an aberration correction technique and high-speed beam scanning technique based on a cutting-edge electron optics system design. Moreover, by combining a high-resolution, large-current beam, it performs high-speed and high-precision inspection measurements while maintaining high resolution within a wide field of view without the need for frequent sample stage movements as in the past. In addition, it uses a dedicated high-speed image processing system for parallel processing of high-speed image capture and image transfer in real time to achieve high throughput with ultra-high-speed data transfer. Furthermore, it also incorporated die to AI (D2AI) inspection[*2] using AI technology to enable high-speed and high-precision recognition of process variations and minute defects.

Hitachi High-Tech will respond to the various needs of semiconductor device R&D and HVM through inspection and metrology systems that apply electron beam technology to continue supporting the evolution of the semiconductor industry.
(Hitachi High-Tech Corporation)

*1 Stochastically induced defects that are attracting attention as a technology issue particularly in the development of EUV lithography technology.
*2 Algorithmic method that inspects part of the wafer area (die) using AI

3 Wafer Surface Inspection System LS9600 Responds to the Need for High-efficiency Inspection

Semiconductor devices for supporting digitization [digital transformation (DX) and IoT], high-speed communications and AI are manufactured with newly designed process manufacturing technology for realizing line widths of 10 nm or less. Semiconductor manufacturing makers require high-speed inspections for particles and defects on wafers with a sensitivity of 20 nm or less to control manufacturing yields during mass production. Wafer surface inspection systems can inspect micro particles and defects using a non-patterned wafer with higher sensitivity and speed, which are difficult to detect on patterned wafers. Regular process monitoring demands for the particles generated from manufacturing equipment are increasing. To respond to process control demand,

3 Wafer surface inspection system LS9600

Hitachi High-Tech Corporation developed and released a wafer surface inspection system, LS9600, which achieves the highest sensitivity of 15 nm (on a bare-silicon wafer) and a maximum throughput of 120 wafers per hour with a newly adopted deep-ultraviolet (DUV) laser and a new optical detection system. In addition, extraction performance of killer defects with an optimized high-precision signal processing algorithm by multi-detection sensors, and a utilization rate of 95% or more in mass production with newly designed laser lifetime prediction technology have been realized. The LS9600 wafer surface inspection system has been introduced to mass production lines for major customers in Europe, North America, and Taiwan for realizing excellent manufacturing quality with reasonable production costs.
(Hitachi High-Tech Corporation)

4 Nanoscale Device Characteristics Analysis System Nano-Prober NP8000

The nanoscale device characteristics analysis system (Nano-Prober) is a scanning electron microscope (SEM) based analysis system that is used to measure the electrical characteristics of transistors and to identify the location of device faults by directly probing the semiconductor device using a microscopic probe with a diameter of several tens of nanometers. With the evolution of semiconductor devices in recent years, the advancement of technology to narrow down fluctuations in the electrical characteristics of devices and the location of faults within circuits due to electron beam irradiation damage have become issues for nano-probers.

The recently developed new Nano-Prober NP8000 achieves high-resolution SEM images under low-acceleration voltage conditions and minimizes the damage due to electron beam irradiation by adopting a new optical system that combines a Schottky electron gun with the boosting deceleration method. In addition, it enables the visualization of low-resistance defects which could not be analyzed with previous equipment by updating the electron beam absorbed current (EBAC)* amplifier function.

Solutions realized with the NP8000 can be expected to be deployed not only for cutting-edge semiconductor device manufacturers, but also for emerging semiconductor companies in China and other fault analysis fields where the demand is likely to significantly increase going forward.
(Hitachi High-Tech Corporation)

* A technology that visualizes fault locations by using a probe to detect and image the current (absorbed current) flowing in a circuit that is generated when an electron beam is irradiated on a semiconductor device.

4 Nanoscale device characteristics analysis system Nano-Prober NP8000