History and Future of Hitachi's Plasma Etching System

Hiromichi Enami Yoshifumi Ogawa Masaru Izawa Takaaki Saito OVERVIEW: Hitachi's etching equipment business has been firmly established since it began research into magneto-microwave plasmas in 1983. This business has continued to expand by developing and implementing superior technologies such as on-board post-etch processing stations and electrostatic chucks. Market requirements have continued to change with each increase in wafer size (200 mm to 300 mm in 2000), the shift in HVM device manufacturing from Japan to Asia, and the continuous reduction in feature sizes predicted by Moore's Law. Hitachi has continued to grow this business by anticipating changes in the market and creating competitive products. For example, Hitachi has been in the forefront of the creation of additional functions that can increase the production efficiency of our etchers. These functionality enhancements have been implemented by some of our customers ahead of the general market resulting in substantial manufacturing advantages. Hitachi will continue to expand this product line in order to meet the requirements for future semiconductor devices which include reducing the impact on the environment.

INTRODUCTION

MANUFACTURING semiconductors such as ULSI (ultra-large-scale integration) chips requires creating multiple levels of patterns on a silicon substrate to form active devices such as transistors, memory elements and wire connections. Each layer of the pattern is formed by a series of steps such as deposition, lithography, etching, and impurity diffusion. In this process, the role of etching is to create the actual pattern by transferring the organic resist pattern formed by lithography to the material(s) below. Technical challenges include the etch rate, selectivity, and dimension control. Performance requirements have become stricter with each successive device generation.

The number of etch process steps is increasing with every generation. Typical devices currently require between 30 and 50 etch steps with minimum processing dimensions in the range of tens of nanometers and more than 10 wire connection layers. Meanwhile, the adoption of new metal materials and three dimensional device structures has resulted in a higher and more exacting level of performance. In the early 2000s, equipment productivity emerged as a key requirement because large memory foundries were constructed during the wafer size transition to 300 mm. As shown in Fig. 1, equipment suppliers are now required to provide solutions to the productivity improvement challenges that customers are facing.⁽¹⁾

HISTORY OF ETCH EQUIPMENT DEVELOPMENT

Full-scale development of Hitachi etching equipment started in 1981 at Hitachi, Ltd.'s Kasadoworks. This was a collaboration between internal semiconductor development and production sites including the Central Research Laboratory, Device Development Center, and Semiconductor & Integrated Circuit Division. It initially led to the development of

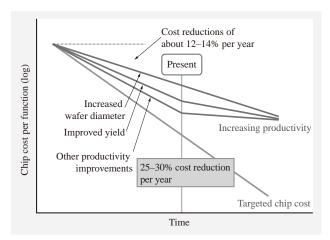


Fig. 1—Tactics for Improving Productivity. The aim is to reduce the functional cost of chips by 25 to 30% per year by reducing feature size, improving yield, and increasing productivity. The measures for improving productivity are the most important.



Fig. 2—Equipment Developed through Special Research Program. A beta tool incorporating a magneto-microwave plasma source was installed at the Device Development Center in late 1984. After design improvements and process evaluation, the unit was re-installed as the first upgraded M-206A in late 1985 (a). The M-308AT was introduced to the market in 1987. Based on the M-206A, it also incorporated further upgrades and an on-board post-etch processing module (b).

batch-type (RE-504) and single-wafer-type (R-206A) parallel plate RIE (reactive ion etching) systems which were the mainstream technologies at the time. This equipment, however, was only used within the company since the performance did not surpass that of competing equipment. Meanwhile, research aimed at supporting a 1.3-µm semiconductor processes, and developing etch equipment for submicron processes started in 1983. The research group developed an etching method characterized by the formation of a high-density plasma (ECR) using the magnetomicrowave technique with independent control of ion acceleration to the wafer using a different highfrequency power source. This ECR system gave a superior etch rate to competing equipment as well as better etch accuracy for policide gate processing. It was first adopted for 1-M DRAM (dynamic random access memory) production and was introduced to the market as the M-206A single-wafer etcher [see Fig. 2(a)]. In the 1.3-µm metal wiring process, a triple-layer structure using a barrier-metal was adopted to prevent aluminum film migration. The ECR system also had significant advantages when used for vertical etching of this structure. This result led to the development of the M-308AT single-wafer etching system which was sold with an additional post-etch processing chamber integrated in vacuum wafer transfer for improved corrosion resistance [see Fig. 2(b)].

Since this time, Hitachi has improved its product development methods to better reflect customer needs while also incorporating new technologies into the equipment based on these two original models. Examples include:

(1) Electrostatic chuck (see Fig. 3)



Fig. 3—Overview of Electrostatic Chuck and Graphic of Reactive Chamber with Electrostatic Chuck.

The electrostatic chuck mechanism played an important role in wafer temperature control but was difficult to install on equipment due to lifetime and damage issues. Despite this, Hitachi was able to develop and commercialize the technology within a year by collaborating with customers and parts suppliers.

This technology improved wafer cooling efficiency significantly by using electrostatic chucking to fix the wafer to the electrode. Hitachi was five years ahead of its competitors in providing a solution which address the potential of charge-up damage.

(2) Time modulation bias

This technology can repeat oscillation in the highfrequency bias for ion acceleration on a time scale of milliseconds. It has been effective for controlling profile and selectivity and has been the subject of continuous improvement.

(3) Low-temperature etching

Low-temperature technology developed at the Central Research Laboratory was further improved and adapted for use in mass production. It is currently used for deep hole and trench processing.

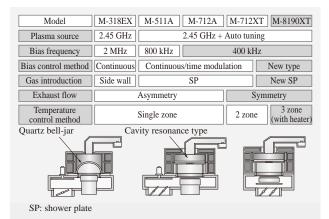


Fig. 4—*Evolution of Magneto-microwave Plasma Use in Silicon Etching Chambers.*

The quartz bell-jar design was adopted for the M-206A and M-318EX and the applied cavity resonance design has been used since the M-511A to improve uniformity on larger wafers. Further improvements were added to improve uniformity and selectivity.



Fig. 5-2010 Etching Equipment Product Range.

The U-8250 dielectric system is used in a wide range of processes. The M-6180 uses the same platform as E-642A and is used for deep hole processing of silicon.

(4) EMCP (electromagnetically coupled plasma)

This uses a unique functional shield technology and achieves good processing characteristics for etching non-volatile materials. The technology was commercialized in the E-series.

All of these technologies have competitive advantages and are currently used in the equipments delivered to the market. Magneto-microwave plasma technology previously developed has seen multiple structural enhancements and additional functions to adapt it for use with different wafer sizes and smaller feature sizes (see Fig. 4). In addition, the ability to perform on-board single wafer wet cleaning was developed and added to the M-308ATW to further improve its anti-corrosion performance after etching corrosive materials. The wet cleaning function is also installed on more recent 500 series models and plays an important role in 200-mm wafer production lines.

HITACHI ETCHING EQUIPMENT PRODUCT RANGE

The current 300 mm capable etching systems, the

M-712XT and M-8190XT, which are sold to large memory and logic fabs as well as foundries, are currently the core of Hitachi's business and have been subject to ongoing improvements (see Fig. 5). Hitachi creates new equipment technologies by providing evaluation machines to customers who develop and produce leading-edge devices and by collaborating with customers on product development^{(2), (3)}.

(1) Co-axial exhaust (see Fig. 6)

This design significantly improves uniformity by placing the electrode co-axially within the etch chamber and by designing the chamber to have a symmetrical shape.

(2) Multi-zone heater electrode (see Fig. 7)

Continuous processing of multi-layer devices requires additional electrode temperature control for each film material. This technology was developed and implemented as a way of quickly increasing or decreasing the electrode temperature.

(3) Multi-wavelength emission detection

This system performs parallel measurements of

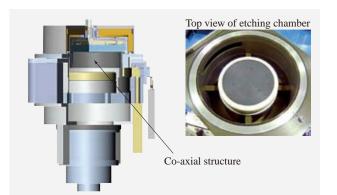


Fig. 6—Structure of Co-Axial Etching Chamber. The symmetric structure includes the wafer transfer path. The inner chamber parts can be easily swapped. CD (critical dimension) uniformity is significantly improved and the CD variation (3 sigma) is less than 3.0–1.5 nm.

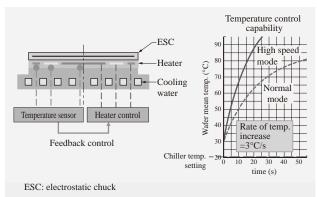


Fig. 7—Electrostatic Chuck Electrode with Three-zone Heater and its Response.

In multi-layer film etching, changing the temperature by layer and by zone in a range from 5 to 20°C improves CD uniformity significantly. In quick control mode, the set temperature is reached in 2 to 6 s. fluctuations in plasma emissions by wavelength. It is capable of detecting small fluctuations that manifest as a shift in emission intensity⁽⁴⁾.

(4) Accurate high-frequency power generator

This features improved linearity in high-frequency output control and provides ion acceleration at low energy. Silicon profile recess was able to be reduced by less than 0.5 nm.

(5) Function to improve wafer edge performance

To prevent a deterioration in performance at the edge of the wafer, this technology improves uniformity by locally optimizing the ion bias energy and gas distribution. It is in practical use. These technical developments also help reduce machine-to-machine differences and time-dependent performance changes by improving process performance including uniformity, multi-layer homogeneity, and profile control.

Joint development work with other equipment suppliers in the important new technology of double patterning has also demonstrated superior process performance (see Fig. 8). The E-541AW and E-642A models have also been produced for use in development focused on the processing of non-volatile materials in which the reaction by-products have a low vapor pressure. These platforms have achieved superior productivity and competitive performance in the production of magnetic heads for HDDs (hard disk drives) and non-volatile memories.

MEASURES FOR DELIVERING ADDED VALUE TO CUSTOMERS

Increasing productivity, equipment availability, and accelerating programs for feature size reduction are major factors in demonstrating to customers the advantages offered by new equipment. As an equipment supplier, it is necessary to implement quick solutions to the following items highlighted in the ITRS (International Technology Roadmap for Semiconductors).

(1) Reduction of CoC (cost of consumables) during operation

(2) Detection and correction of time-dependent performance changes

(3) Detection and correction of machine-to-machine differences

(4) Reduction of non-production wafer processing

(5) Establishment of reactive chamber cleaning methods and associated checking methods

(6) Establishment of equipment maintenance methods and associated rules

For time-dependent performance changes and

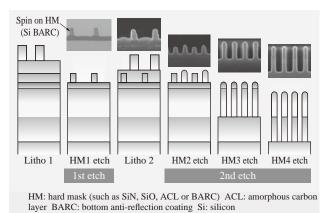


Fig. 8—*Example of Double Patterning Using M-8190XT [LELE (Litho-etch-litho-etch Method)].*

The second lithography step creates a pattern between the pattern created in the first lithography step. By adjusting the selectivity when processing each layer, the final patterns (after HM4 etching) can be made to be very similar.

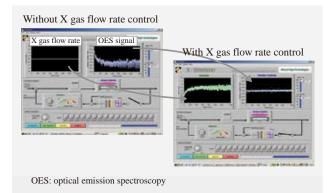


Fig. 9—Example of Practical Use of EPC (Equipment Process Control) System.

The technology is used to improve CD and selectivity control for 65-nm and later device generations.

machine-to-machine differences, measures need to be implemented in the equipment itself. One example is the EPC (equipment process control) system (see Fig. 9). This system uses an equipment gas monitor to measure a sensor value that has a close relationship to critical feature dimensions and selectivity. These items are key parameters for process performance. The equipment controls the critical value by adjusting the gas flow. One example application involved a processing cycle of 100 dummy wafers followed by 500 product wafers and equipment cleaning. Introducing the system allowed the customer to improve the procedure to five dummy wafers followed by 15,000 product wafers and achieved an 18% increase in equipment availability.

Year		2008	2009	2010	2011	2012	2013
Trend (R&D)	MPU-PGL	24	22	20	18	17	15
	NAND 1/2 pitch (un-contacted poly)	38	32	28	25	23	20
	DRAM 1/2 pitch (contacted)	52	45	40	36	32	28
hp-LSI technology node (R&D)		32 nm	22 nm		15 nm		11 nm
	CDU (3o)	1.4	1.3	1.2	1.1	1.0	0.9
Technology roadmap	Lithography	ArF immersion with water Double patterning (LELE/LPLE) 2 step trim LWR reduction					
	Gate etching Flash memory DRAM	•Fin-FET for memory •Fin-FET for logic					lear mid-gap /F pased HM
	BEOL etching	Metal hard mask + ultra low-k MIMO R2R control					
	System	•FDC •OCD FF/FB					L

MPU-PGL: microprocessing unit—physical gate length hp: high performance CDU: critical dimension uniformity EUV: extreme ultra violet SADP: self-aligned double patterning LPLE: litho-process-litho-etch LWR: line width roughness Fin-FET: fin field effect transistor MG: metal gate WF: work function electrodes HM: high mobility HARC: high aspect ratio contact BEOL: back-end of line FDC: fault detection & classification OCD: optical critical dimension MIMO: multiple-input multiple-output

Fig. 10—Trends for Future Devices and Key Processes. The table contains Hitachi High-Technologies Corporation's own predictions for trends in devices and key processes based on feedback from customers and seminars.

CONCLUSIONS

As shown in Fig. 10, it is important that etching equipment address major issues such as: (1) continuous reduction in feature size and associated uniformity issues, (2) larger wafer sizes (450 mm), (3) evolution of three-dimensional devices, (4) adoption of new materials, and (5) future lithography technologies such as EUV (extreme ultraviolet). It is absolutely necessary to also continue to reduce the inevitable machine-to-machine variations and time-dependent performance changes as described earlier in this article. Finally, environmental measures, including energy savings, have also become one of the major points in selecting equipment suppliers. Hitachi will continue to work with its customers and suppliers to consider solutions and implement them in a timely manner.⁽⁵⁾

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ABOUT THE AUTHORS



Hiromichi Enami

Joined Hitachi, Ltd. in 1978, and now works at the Semiconductor Manufacturing Equipment Division, Electronic Device Systems Business Group, Hitachi High-Technologies Corporation. He is currently engaged in sales and marketing of semiconductor processing equipment. Mr. Enami is a member of the Japan Society of Applied Physics.



Yoshifumi Ogawa

Joined Hitachi, Ltd. in 1981, and now works at the New Product Development Group, Kasado Design & Production Division, Electronic Device Systems Business Group, Hitachi High-Technologies Corporation. He is currently engaged in design and process development of future dry-etch equipment. Mr. Ogawa is a member of the Japan Society of Applied Physics.



Masaru Izawa

Joined Hitachi, Ltd. in 1989, and now works at the Department of Nano-Process Research, Central Research Laboratory, Hitachi, Ltd. He is currently stationed at the Kasado Design & Production Division of Hitachi High-Technologies Corporation and engaged in the development of future dry-etch equipment. Mr. Izawa is a member of the Japan Society of Applied Physics, and the Chemical Society of Japan.



Takaaki Saito

Joined Hitachi, Ltd. in 1991, and now works at the Semiconductor Manufacturing Equipment Division, Electronic Device Systems Business Group, Hitachi High-Technologies Corporation. He is currently engaged in marketing and strategy formulation for semiconductor processing equipment.