FOR IMMEDIATE RELEASE

Cloud-based verification simulation technology to analyze the effect of semiconductor memory error on industrial equipment and vehicular control

Tokyo, Japan, 2nd December 2011 – Hitachi, Ltd. (NYSE: HIT/TSE: 6501, hereafter, Hitachi) and Kobe University today announced the development of a cloud-based simulation technology for verifying effects caused by failure in semiconductor memory devices used in electronic control units (ECUs) installed in industrial equipments, automotive vehicles, and robots. This technology makes it possible to verify on a computer various effects caused by semiconductor-memory failure in cases such as embedded software and hardware like engines and motors. Moreover, applying it to development of ECUs makes it possible to verify the effect of the semiconductor-memory failure in a short time. Furthermore, the technology makes it possible to reduce the risks caused by the semiconductor-memory failure (such as an entire system going down). The developed simulation technology enables effective development of control units based on functional safety(1).

The developed simulation technology integrates Hitachi's virtualized hardware-in-the-loop simulation (vHILS)(2) technology and Kobe University's memory-device simulation technology. To integrate these two technologies, two techniques were developed: a fault-case generator and cloud-based parallel computing. The fault-case generator generates memory-failure data patterns according to various device parameters such as supply voltage, operating temperature, and process variation, and it then inputs the generated memory-failure data patterns into the vHILS. The cloud-based parallel computing concurrently calculates the effect of each memory-failure pattern by automatically allocating a large number of memory-failure patterns to a number of calculation nodes in the cloud. To evaluate the developed technology, it was used to simulate an ECU-system-embedded 1-Mbit SRAM by using 600 calculation nodes and a communication cycle of 10 milliseconds. The evaluation results suggest that 670,000 memory-failure patterns (equivalent to 6000 semiconductor memory chips) can be simulated in about 12 hours.

The technology was developed for supporting "Dependable SRAM(3) Techniques for Highly Reliable VLSI System (Principal Investigator: Professor M. Yoshimoto, Kobe University)", which is a research challenge for "Fundamental Technologies for

Dependable VLSI Systems (Research Supervisor: Dr. S. Asai)" within Core Research for Evolutional Science & Technology (CREST), promoted by the Japan Science and Technology Agency. By applying the developed simulation technology to an ECU-system-embedded dependable memory developed by Kobe University, reliability of the ECU system was evaluated. The evaluation results confirm that the simulation technology can predict effects (such as an abnormal termination of a system) caused by the semiconductor-memory failure.

With the advances in functionality of industrial equipments, automobile vehicles, and robots, it is required to enhance energy conservation and production efficiency. In addition, the amount of embedded software implemented in an ECU has increased; therefore, reducing development cost and shortening development period have become major issues. Moreover, as efforts aimed at enhancing safety of the control units that use electronic devices and computers, functional safety standards have recently been introduced to cover such control units; consequently, responses to these standards have also become major issues. A lot of semiconductor devices (including microprocessors) are used in an ECU. With the advance of semiconductor microfabrication technologies, incorrect operation of semiconductor devices (due to disturbances such as electrical noises and cosmic rays as well as aging) is a growing concern. Accordingly, as for ECU development, measures to prevent microprocessor failure are also major concerns. In particular, since computer memory uses a lot of semiconductor devices, the flow of the control program changes according to whether a failure is generated in the semiconductor device (namely, address-position-information error) or whether an error is generated in the embedded software (namely, time-information error). According to the change of flow, operation of plants to be controlled by the ECU, as well as operation of the ECU itself, changes. Furthermore, to design a reliable system, functions of the embedded software affected by the various semiconductor-memory failures must be evaluated. It is, however, difficult to experimentally verify various functions. The aim of this work was therefore required to develop a simulation technology that can assess and verify various effects caused by semiconductor-memory failure in the case of embedded software and hardware such as engines and motors.

In response to this need, a cloud-based verification simulation technology that integrates Hitachi's vHILS and Kobe University's memory-device simulation technology was developed. This simulation technology can effectively verify on a computer various effects caused by various failures in semiconductor memory devices used in ECUs in the case of embedded software and hardware such as plant.

Details of the developed technology are described below.

(1) Fault-case generator: a bridge between a memory-device simulation and a virtualized hardware-in-the-loop simulation

The fault-case generator was developed to input a transistor-level semiconductor-memory-failure data pattern into an internal-memory model in the ECU model in the vHILS. Basic causes of a memory failure are calculated by the memory-device simulation. The memory-failure data patterns generated according to verification conditions for the vHILS are input into the internal-memory model by the fault-case generator. (The verification conditions include arbitrary waveforms for power-supply noise, operating temperature, and aging.) The generator can input a large number of memory-failure data patterns into the vHILS; thus, several tens of thousands of semiconductor memory chips (equivalent to a large number of memory-failure data patterns) can be verified via simulation.

(2) Cloud-based parallel computing: Verification of a large number of memory-failure patterns can be automatically performed in a short time.

Cloud-based parallel computing was developed to reduce simulation time by means of massively parallel-computing in a cloud-computing environment. The developed cloud-based verification simulation technology can concurrently analyze the effect of each memory-failure pattern by allocating a large number of patterns to a lot of calculation nodes in a cloud. Moreover, it can automatically analyze the results. It can thus assess the effects of a large number of memory-failure patterns in a short time.

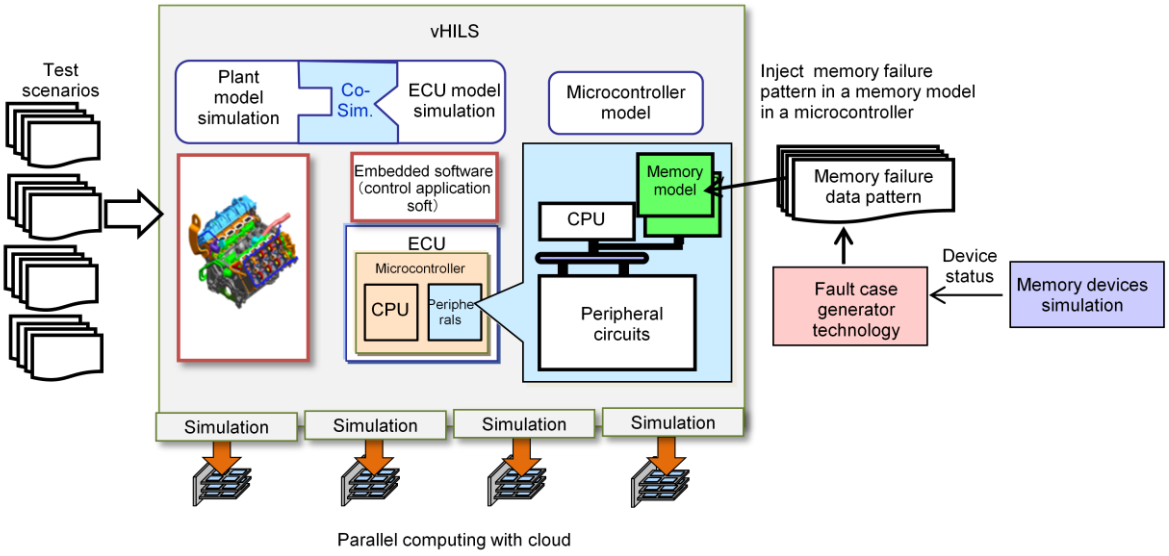
These results will be presented on 3rd December 2011 at the Dependable VLSI Systems Workshop 2011/12, which will be held at the Takeda Hall, Hongo Campus of the University of Tokyo, Tokyo, Japan.

Notes

(1) Functional safety: An attempt to enhance the safety of equipment. By calculating the risks of failure of parts making up equipment in advance, various safeguards to reduce the risks can be installed in the equipment.

(2) Virtualized hardware-in-the-loop simulation (vHILS): Compared to hardware-in-the-loop simulation technology that verifies an embedded software by combining a simulation model of components(which is subjected to evaluation) with a real ECU, vHILS technology can verify control software by modeling ECUs without the need for hardware.

(3) Dependable SRAM: Compared to a conventional memory device, a dependable SRAM is not sensitive to disturbances (high frequency) such as electrical noises and cosmic rays. This feature substantially reduces the number of read/write/hold failures. A dependable SRAM is therefore a highly reliable memory.



About Hitachi, Ltd.

Hitachi, Ltd., (NYSE: HIT / TSE: 6501), headquartered in Tokyo, Japan, is a leading global electronics company with approximately 360,000 employees worldwide. Fiscal 2010 (ended March 31, 2011) consolidated revenues totaled 9,315 billion yen ($112.2 billion). Hitachi will focus more than ever on the Social Innovation Business, which includes information and telecommunication systems, power systems, environmental, industrial and transportation systems, and social and urban systems, as well as the sophisticated materials and key devices that support them. For more information on Hitachi, please visit the company's website at http://www.hitachi.com.

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