ASIC Technology for the Implementation of System-on-a-Chip

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ABSTRACT: The rapid advances in multimedia technology—together with current computer, communications, and consumer-oriented media technology—are having a major impact on our everyday lifestyle. This trend has been largely due to recent advances in emerging VLSI and ULSI semiconductor technology. Multimedia products need to provide high-performance capabilities at low-power dissipation levels in compact packages at affordable prices. The application of semiconductors, however, poses a few technically contradictory problems. These technological issues can be resolved using application specific IC (ASIC) technology with its ability to implement the so-called system-on-a-chip. The many hi-tech appliances that surround us today — like the handheld computers, car navigation systems, digital cameras, computer games, and the ubiquitous cellular phones — owe their existence to this emerging ASIC technology. Hitachi is fully committed to the system-on-a-chip design paradigm through the promotion of the embedded microprocessor ASIC, known as the μCBIC (micro-cell-based IC), with support for CPU cores for the SuperH and H8 microprocessor series plus a plethora of analog circuit blocks and other intellectual property (IP) modules. Our current flagship product, the DRAM-ASIC, is also making new in-roads into the multimedia marketplace. Our newest standard cell product, the HG75C Series, shipped recently and is based on the state-of-the-art 0.18-μm process technology. In the future new products with this advanced process will be released as μCBICs or DRAM-ASICs, or both.

INTRODUCTION

THE demand for higher functionality and technical complexity, and the implementation of smaller device size and lower power dissipation, present demanding technological challenges that need to be resolved for the emerging multimedia and portable markets. Today, a major problem is how to deal with time-to-market cycles (sales cycles) due to shorter product lifetimes and shorter design and development cycles.

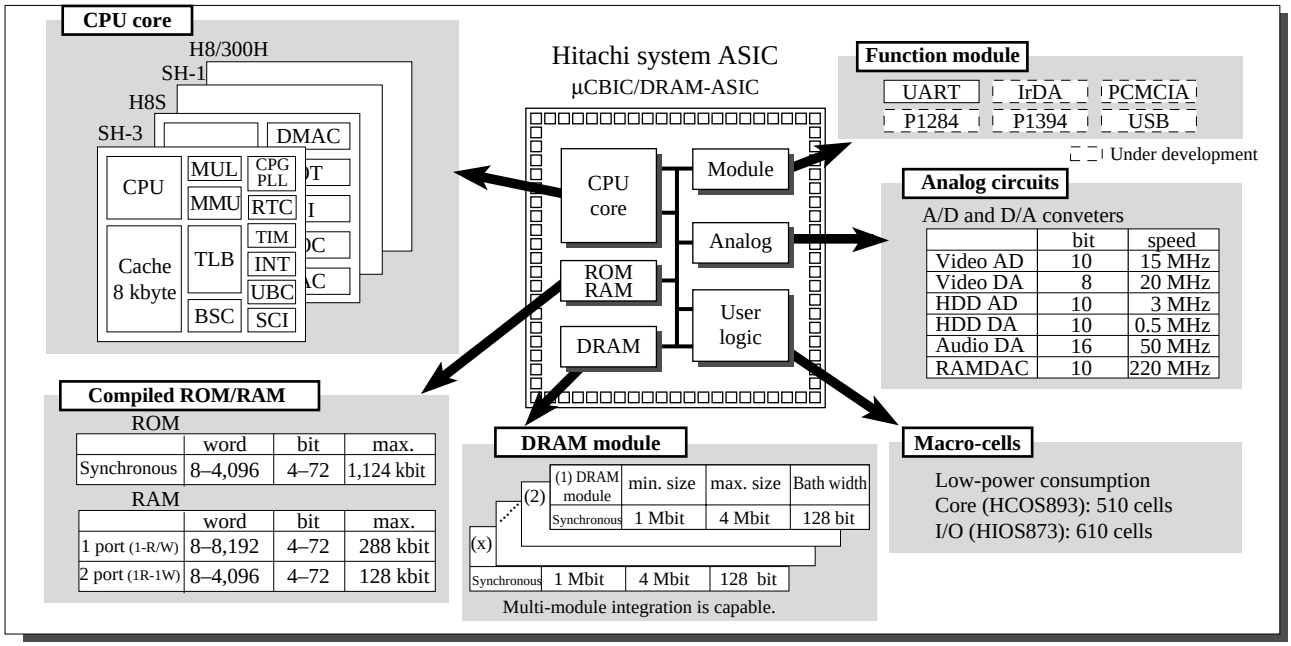
The solution is already here in the form of the system-on-a-chip ASIC fully capable of integrating microprocessor, memory, and analog circuits — and gate-array elements — all on a single chip. The main characteristics of these highly flexible ASIC products are value-added features like highly functional performance and high operating speed.

Innovation in ASIC technology is closely linked to the evolution of process technology. In the past, we advanced from 3-μm gate arrays to 0.8-μm cell-based ICs with on-chip compiled RAM and ROM memory. Then, at the 0.5-μm process level, we introduced a CPU core-based ASIC with embedded analog circuits that integrated a 32-bit reduced instruction set computer (RISC) core together with analog-to-digital converter (ADC) and digital-to-analog converter (DAC) modules. At 0.35-μm, the trend is to integrate dynamic RAM (DRAM) with logic on a single chip. With the state-of-the-art 0.18-μm process technology, the micro-cell-based IC (μCBIC) and the DRAM-ASIC will be fully enhanced to provide the system-on-a-chip solutions shown in Fig. 1.

In this article, we discuss the salient features, superiority, and future prospects of the μCBIC and the new DRAM ASIC and Hitachi system-on-a-chip paradigm.

EMBEDDED-MICROPROCESSOR CELL-BASED IC (μCBIC)

The system-on-a-chip is indispensable for the implementation of the highly functional, compact integrated circuits used in today's electronic products. The CPU core, in particular, is the main technology



CPU: central processing unit
MUL: multiplier
MMU: memory management unit
TLB: translation lookaside buffer
BSC: bus controller
CPG: clock pulse generator
PLL: phase-locked loop
RTC: real-time clock
TIM: timer
INT: interrupt controller
SCI: serial communication interface
DMAC: direct access controller
ROM: read-only memory
µCBIC: micro-cell-based IC
RAM: random access memory
DRAM: dynamic RAM
AD: analog-to-digital
DA: digital-to-analog
UART: universal asynchronous receiver/transmitter
IrDA: Infrared Data Association
PCMCIA: Personal Computer Memory Card International Association
USB: universal serial bus
HDD: hard disc drive
RAMDAC: RAM digital-to-analog converter
UBC: user break controller
R: read
W: write
I/O: input-output

Fig. 1—Hitachi System ASIC.
The µCBIC, using the SuperH and H8 series of CPU cores, implements full microprocessor customization, integrating high-speed high-accuracy analog circuits, functional modules, compiled memory, and user-defined logic. The DRAM-ASIC integrates high-density DRAM memory together with the functionality of the µCBIC using optimized merged process technology.

feature that needs to be determined at the outset of the system design. It is usually a standard CPU core based ASIC, developed originally as a proprietary stand-alone part that integrates as much functional diversity as possible, including some functions potentially superfluous to system design, to provide a general-purpose performance capability. On the other hand, system functions that may be lacking, often have to implemented with a two-chip design using a gate-array type element.

An important factor in implementing the system-on-a-chip is the ability to customize a diversified range of user-specified CPU-based functions in as short a turnaround time as possible. Also, because of the specialized knowledge requirements about specific microprocessor bus specifications needed to route CPU core and associated peripheral interconnects, design was traditionally considered a nontrivial task for the individual user. To ease the burden of the user's design tasks and reduce design and development time cycles, Hitachi developed a CPU compiler capable of automating the routing between the CPU core and associated peripheral modules.

CPU Compiler

The CPU compiler, which is an interactive menu-driven design automation (DA) tool, installed to run on the user's workstation, is used to select the modularized CPU core and peripheral logic components needed to implement the user's design intent. The compiler uses the selected CPU core and associated peripheral modules to create the netlist and top-level symbol, once the modules have been routed, as shown in Fig. 2.

Using interactive menu selection, the user first selects the standard microprocessor that will form the basis of the system design. Then, only those functions needed to satisfy the design intent are selected, module

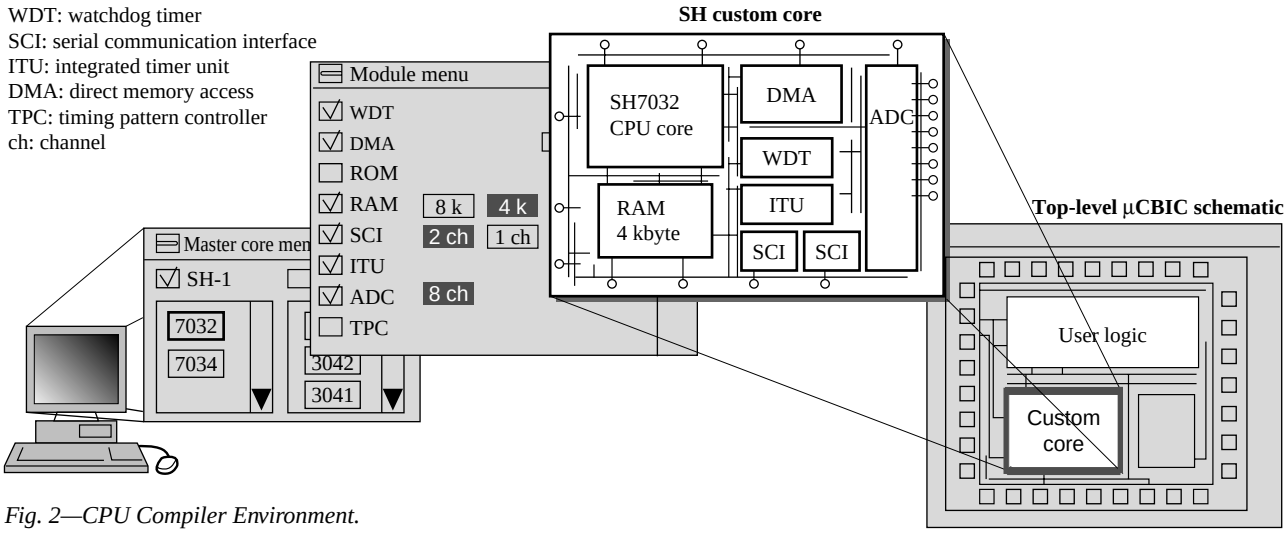


Fig. 2—CPU Compiler Environment.
The CPU compiler is a Hitachi propriety DA tool that automatically genertes the custom core (CPU) netlist based on a customized core specification, the simulation model, and test vector data for custom-core level verification by selecting specific modules from the compiler's interactive menu.

by module, from among the peripheral functions associated with the selected CPU. In particular, the user can select the required number of modules used for direct memory access (DMA), and the number of analog input channels for A/D conversion. Also, fixed-capacity RAM/ROM modules that directly interface with the CPU can be selected in memory configurations equivalent to the standard stand-alone microprocessor.

CPU Core

Efficient chip-level verification is essential for LSIs with an embedded microprocessor. Chip-level verification is adequately handled using a library of preverified CPU-core and associated peripheral modules. Quick and flexible logic verification can be

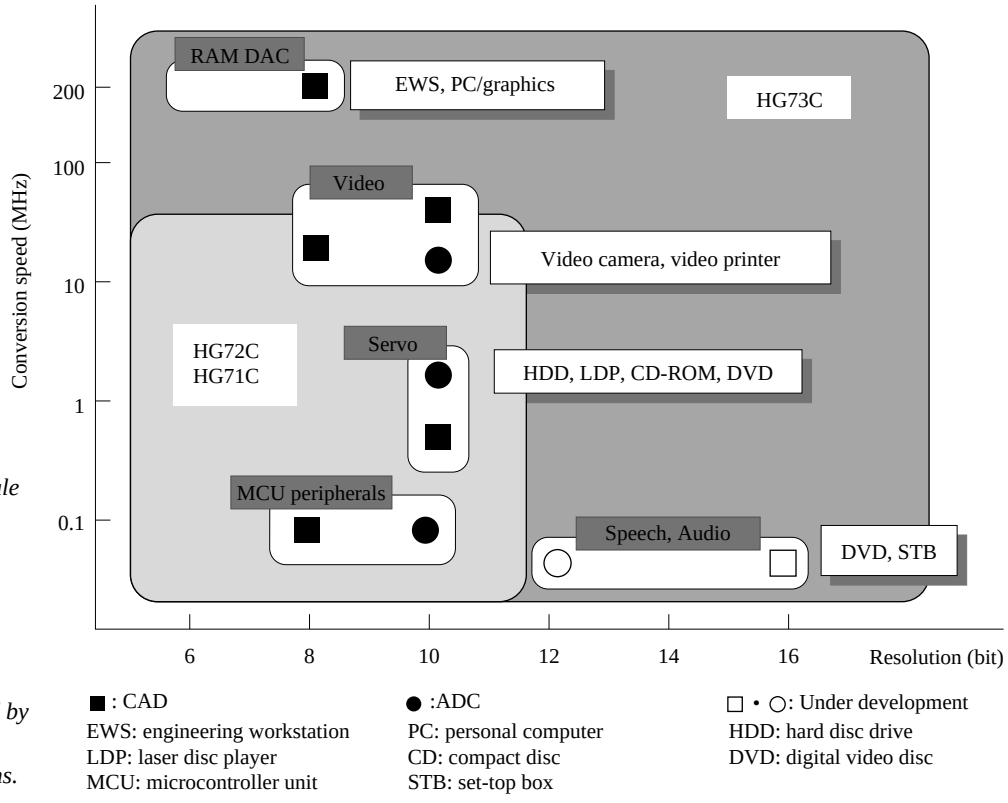


Fig. 3—μCBIC Analog Module Development.
Analog modules include A/D and D/A converters for video and servo applications and RAMDACs for graphics applications. This analog lineup will soon be enhanced by a high-accuracy module for speech and audio applications.

performed by integrating the various modules on chip as a preverified library of cell functions.

In particular, the provision of circuits that exhibit characteristics sensitive to certain aspects of the design, such as analog circuits, as a library of preverified modular building blocks vastly reduces verification time cycles. Also, the availability of logic models and standard test vectors for all CPU-core and peripheral modules substantially reduces user simulation time and the burden of test vector design.

Hitachi has been expanding its inventory of CPU cores for the SH family and H8 microprocessor series for application in the HG71C, HG72C and the HG73C Series, currently in mass production. In the future, the HG75C Series, shipped recently without available CPU cores, will implement CPU cores of the SH family as the μCBIC-like HG71C, HG72C and HG73C Series.

Analog Modules

Special-purpose analog circuits, indispensable to full implementation of the system-on-a-chip solution, can be interconnected using the CPU's external bus interface (Fig. 3). Hitachi supports a rich variety of A/D and D/A converter modules optimal for use in video, servo-control, and microprocessor peripherals. In addition to the low-voltage versions of the analog modules currently available, high-accuracy voice/audio-oriented and ultrahigh-speed graphics-oriented analog modules are currently in the development stage.

Compared with conventional digital circuits, analog circuits need longer simulation times. As a result, LSIs with mixed on-chip analog and digital circuit blocks are very difficult to verify within practical time frames. A solution to this problem is to provide each A/D and D/A converter module with a pseudo logic model. This enables mixed analog and digital simulation to be performed at speeds on a par with purely digital modules.

User Logic Design

A top-down design methodology, based on high-level behavioral languages such as Verilog-HDL (hardware description lnguage) and VHDL (very high speed integrated circuit hardware description language), is essential for logic designed in-house by the user.

Hitachi provides support for an optimized library of synthesized logic cells. This library is designed to provide the most efficient method for high-density conversion by converting the logic defined in terms of a high-level behavioral language to the gate level by logic synthesis. The μCBIC example in Fig. 4 shows a chip micrograph with integrated SH-1 CPU core.

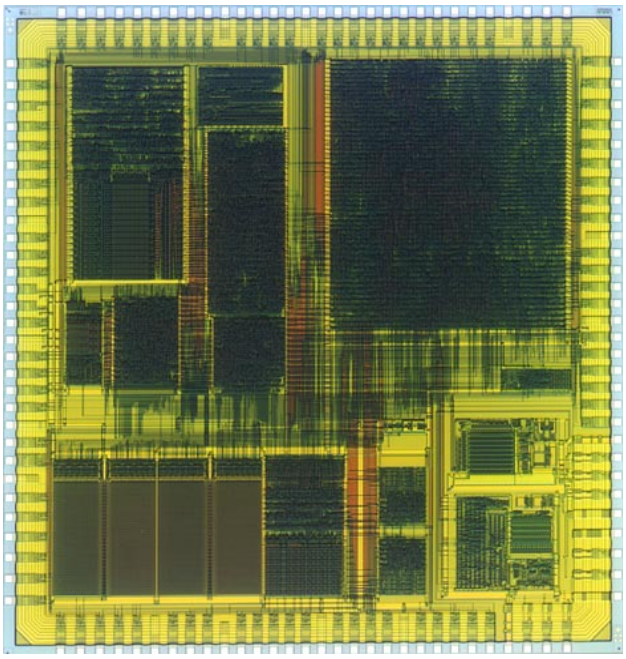


Fig. 4—μCBIC Design Example.
The figure shows the micrograph of an HG72C Series chip design integrating an SH-1 CPU core, high-speed A/D and D/A converter modules, memory and 20-kgates of user logic.

DRAM-ASIC

In the multimedia arena, personal handy data systems, image and video processing, and cache systems need vast amounts of memory to cope with the huge data throughput that needs to be processed. We can also cite the never-ending demand for higher functional performance, smaller package sizes, and lower power consumption levels.

In conventional systems that interface with external standard DRAM, the restricted printed-circuit board (PCB) space available for data-bus expansion (more than 64 bits) made it difficult to implement high-speed data transfers. Also, the high bus loads that the PCB had to drive were an additional bottleneck to reducing power consumption levels.

The wisdom of integrating DRAM on the same silicon wafer is reflected not only in the PCB space savings resulting from fewer components, but in higher data transfer efficiency due to a simplified data-bus expansion (from 64 to 128 bits) capability, and the lower power dissipation levels that arise from reduced bus-drive current levels (Fig. 5).

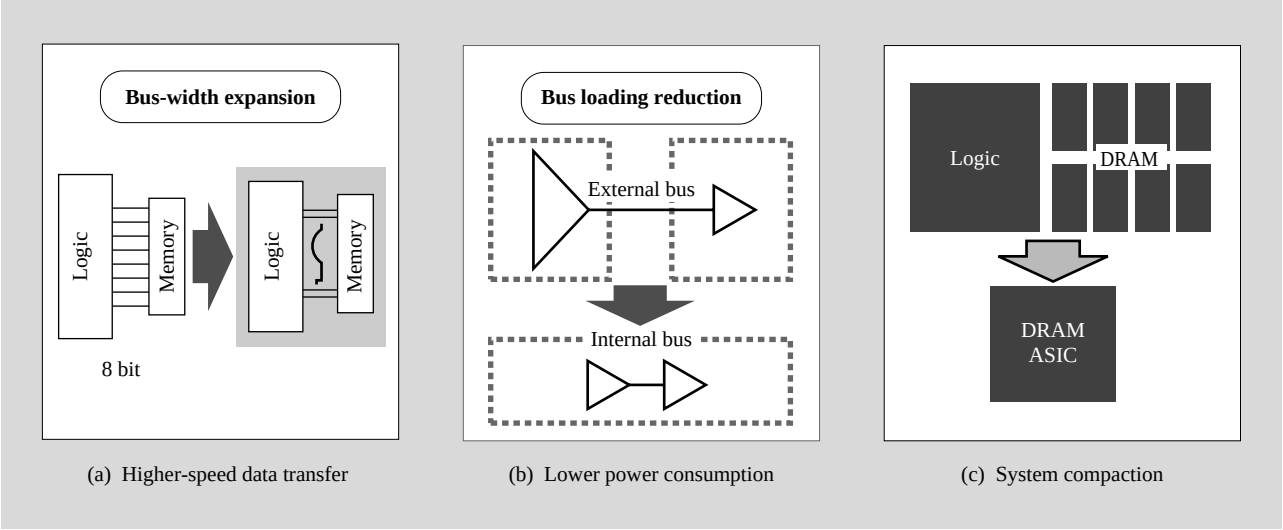


Fig. 5—Merits of the DRAM ASIC.
Integrating DRAM and logic on a single chip provides the following merits: (a) high-speed data transfers thanks to a simplified bus expansion capability, (b) lower power consumption due to reduced bus loading, and (c) system compaction.

DRAM-ASIC Process Technology

DRAM fabrication employs three 'tried-and-tested' memory-cell process methods: the planar method, the trench method, and the stack method — each with its own merits and demerits. The planar method, which provides the best compatibility match with the logic process, is ill-suited to high-density integration. The trench method, while providing optimum logic performance and a high level of surface flatness, falls short of the stack method in terms of integration density, because of the need to implement logic isolation.

The stack method is unsurpassed in terms of high-density integration, but suffers from degradation of logic characteristics due to the fact that the memory-cell heat-treatment process takes place after MOS logic fabrication. However, thanks to recent innovations in low-temperature process technology, this difference has been substantially reduced, even compared with the trench method. Thus Hitachi produced the HG73M series of ASICs with the ability to integrate high-density DRAM, without compromising logic performance, thanks to the adoption of the stack method.

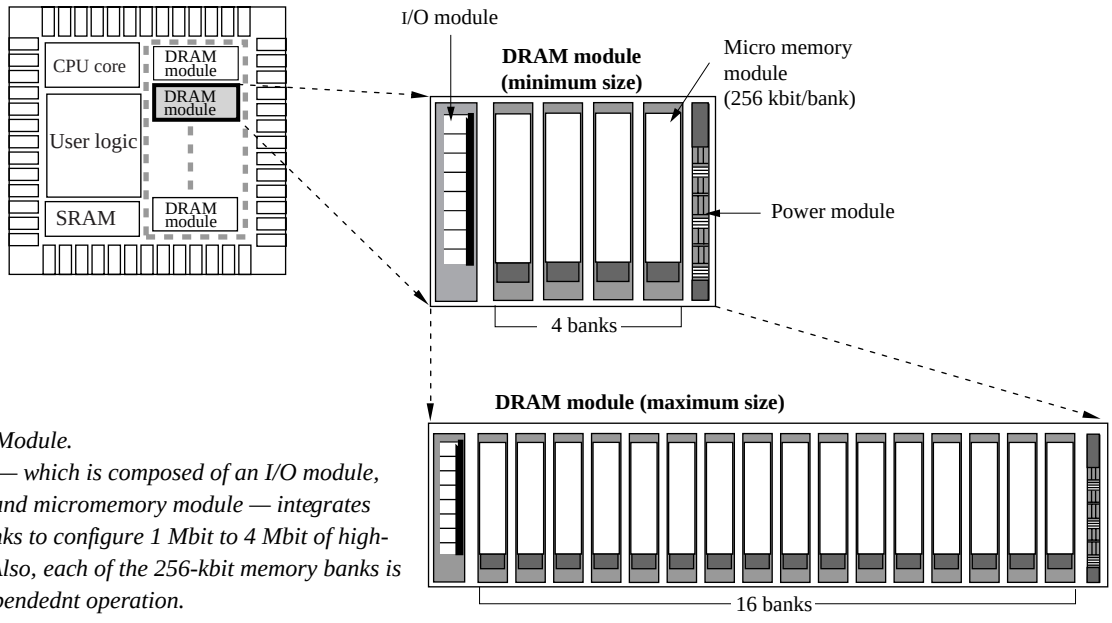


Fig. 6—DRAM Module.
DRAM Module — which is composed of an I/O module, power module, and micromemory module — integrates from 4 to 16 banks to configure 1 Mbit to 4 Mbit of high-speed DRAM. Also, each of the 256-kbit memory banks is capable of independednt operation.

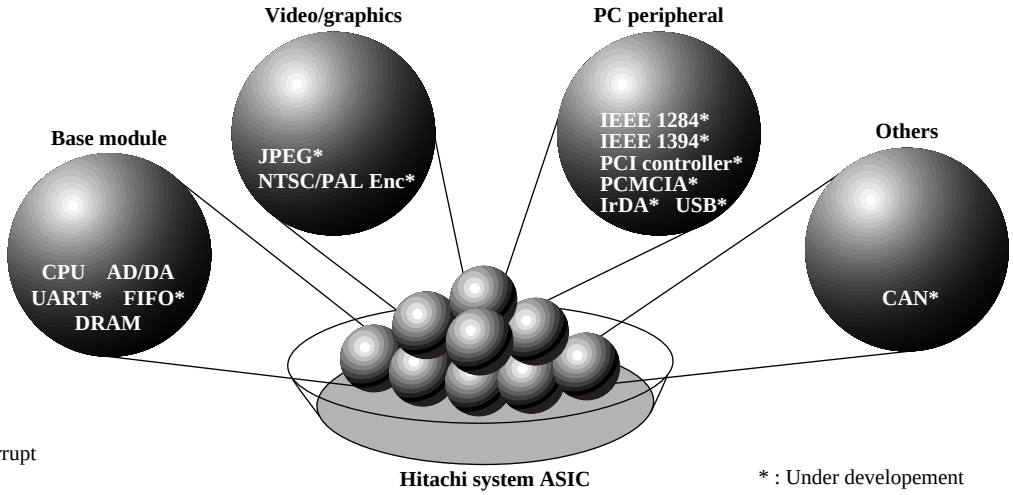


Fig. 7—AS Module Enbedded System ASIC Development Plan.
Application specific (AS) modules, also kown as intellectual property (IP) modules, are becoming indispensable technological elements in system-on-a-chip designs such as system ASICs.

DRAM Micromodule Architecture

In the HG73M Series, the logic half of the chip is based on 0.35-μm CMOS cell-based IC technology using the same cell library as used in the HG73C Series. With the DRAM modules of the chip, which supports a high-level language model, users can perform mixed DRAM-logic simulation on their own in-house workstations following customization of the DRAM micromodule bus-width and bank-configuration requirements.

By adopting the micromodule-architecture, the DRAM module simplifies integration of large-scale memory with flexible organizations. The micromodule architecture is a design methodology in which memory expansion is performed using banks based on a standard 256-kbit, clock-synchronous DRAM memory block. For example, a 4-Mbit DRAM configuration can be implemented using 16 memory banks (Fig. 6).

As for DRAM speed, the adoption of a multibank, cascaded memory-access pipeline and 128-bit wide data bus vastly improves the efficiency of the data transfer rate. These devices are also capable of 16-, 32-, and 64-bit wide configurations.

Also, with application of optimized process technology, the functional performance of the logic is able to keep pace with the high-speed capability of 0.35-μm technology up to a maximum of 150 MHz.

Since the bus lines driving the DRAM and logic are internal to the system, the lower bus-drive current and hence reduced bus loading results in lower power consumption levels compared with conventional system board designs.

AS MODULE EXPANSION

Recent user demand for system-on-a-chip products has spurred silicon vendors into providing a plethora of new application specific (AS) modules, also known as intellectual property (IP) modules, that are finding wide use in video and computer applications.

Hitachi is currently developing products for Joint Photographic Experts Group (JPEG) NTSC/PAL encoders, RAMDAC used in still picture and video applications; also computer peripheral implementations of the following standards: IEEE P1284/P1394; Universal Serial Bus (USB); Peripheral Component Interconnect (PCI) bus; Personal Computer Memory Card International Association (PCMCIA)interface, and Infrared Data Association (IrDA) interface — as shown in Fig. 7.

ASIC DESIGN ENVIRONMENT FOR FAST DEVELOPMENT CYCLES

The need to reduce user design work loads for the development of functionally complex ASICs integrating CPU core, analog blocks, and IP modules on a single chip is discussed here.

System Design and Logic Verification

System-on-a-chip design requires mixed-level simulation for modules defined in terms of VHDL or Verilog-HDL. To meet these needs, electronic design automation EDA tool-kit vendors are currently shipping design kits, focused on function-level simulators, capable of handling both behavioral language formats.

Also, with the improved integration densities achieved as a result of fine-pattern process technology, the question of exceptionally long timing verification times due to the huge amounts of test vector data for simulation needs to be resolved.

With ever increasing circuit logic densities, systems capable of reducing logic verification times based on a combination of a cycle based simulator that verifies only logic functionality while ignoring timing delays, and a static timing analyzer that verifies logic circuit timing under static conditions without invoking logic simulation, will become the norm in the near future.

Software Development Environment

Microprocessor-based LSI design requires the support of emulators that provide software development and system debug support capabilities. A dedicated CBIC simulation board also needs to be built in order to flexibly cope with the variety of on-chip modules and wide range of different user logic designs. Integrating evaluation EVA chips for the analog modules and gate-arrays and field programmable gate arrays (FPGAs) for the user logic expedite emulation of the LSI target image. Also, the introduction of codesign environments that support both hardware design and software development on the same workstation is needed.

Design for Testability

Design for testability is an important phase of ASIC design. In the μCBIC design, multiplexing circuits are adopted for CPU core and peripheral module testing. For user logic testing, the shift-scan method is employed.

With the multiplexing method, MUX circuits are inserted to logically isolate the individual function modules from the other on-chip blocks, enabling the LSI to be tested from the external I/O ports. In addition, control circuits exhibiting external observability and controllability that also perform simultaneous test-vector conversion, are inserted around the periphery of the functional modules.

With the shift-scan method, scan flip-flop insertion and the addition of the control logic used to control data scan-in and scan-out are fully automated as is test vector generation. Fault coverage currently achieves detection rates of 99%, and higher.

CONCLUSIONS

This paper discusses the microprocessor-based ASIC μCBIC and embedded-DRAM ASIC, two major products of Hitachi System ASIC. Hitachi has established the design technology needed to implement the system-on-a-chip solution. The most outstanding feature of this design technology is the way it simplifies user logic design and substantially reduces development time cycles. In the future, enhancements such as leading-edge CPU cores, analog circuitry, and a full IP-module lineup, together with high-density DRAM and flash memory merged on a single chip will be introduced to meet the ever-diversifying needs of the discerning user.

Hitachi's advanced process technology, such as 0.18 μm and finer, will accelerate the enhancements leading the way in the age of the system-on-a-chip solutions.

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