

SuperH RISC Engine Chip Set for Handheld PC

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*ABSTRACT: Mobile computing devices such as HPCs (handheld PCs) with Windows*1 CE and PDAs (personal digital assistants) are gaining popularity for personal information management and easy connectivity with PCs. Battery life is important for these devices. Thus the microprocessor used must feature low power as well as high performance. New peripheral functions such as color display support are also becoming popular. Hitachi has been developing the SuperH RISC (reduced instruction set computer) engine microprocessor series and companion chips to support the multifaceted requirements of mobile computing devices. Color display, fast IrDA (Infrared Data Association), compact flash, and modem communications are supported by Hitachi's chip set.*

INTRODUCTION

IN the fall of 1996, a new OS named "Windows CE" was announced by Microsoft Corporation, and seven companies started to sell HPCs that run this new OS. These HPCs are small and portable information instruments, and they can be powered by batteries for many hours. This high level of performance is based on the evolution of microprocessor and the software technology. To meet the demands for a higher performance, lower power consumption, higher functionality small size microprocessor, Hitachi is developing the SuperH RISC engine family that implements both high-speed microprocessor technology and low-cost microcontroller technology. This review describes the SuperH RISC engine family, especially the functions and specifications of the SuperH engine for Windows CE.

SUMMARY OF SUPERH RISC ENGINE FAMILY

The SuperH RISC engine family lineup has been expanding to meet the various system requirements of performance, power consumption and price in applications such as mobile computing device processors and embedded controllers. By adopting RISC architecture, the CPU core size is made very small. This enables Hitachi to put a cache memory and many peripheral circuits on a very small chip. The family provides glueless interface circuits to

DRAM (dynamic RAM) and other memories. Thus systems can be built with few additional parts.

Because the SuperH RISC engine family's operation code is 16-bit fixed length and other RISC architectures use 32-bit fixed length code, systems can reduce the memory size needed to store operation codes. Thus system price is reduced. More instructions can be stored in cache memory and the cache hit ratio is increased to improve the system performance. Fig. 1 shows the lineup of the SuperH RISC engine family. There are four types of CPU, from the SH-1 which operates at 26 MIPS to the SH-3 which runs at 120 MIPS, and the SH-DSP which has DSP class multiply-add arithmetic performance. In addition, the 360-MIPS SH-4 is being developed.

The first product, the 26-MIPS SH-1, is a single chip microprocessor with ROM and RAM. On-board peripherals include a direct interface to DRAM, DMA (direct memory access) controller, multifunction timer, serial interface, and A/D converter. These modules make it possible to use this RISC microprocessor in embedded applications. There have been many design wins in various applications such as motor controllers and car navigation systems.

The second product, the 37 MIPS SH-2, has a 4-kbyte cache memory. Peripheral functions include DMAC (DMA controller), serial interface, timer, and a direct memory interface for connection to DRAM and SDRAM (synchronous DRAM). It is used for video game machines and Internet TVs. There are eight single chip type products that have the SH-2 as the CPU core — such as the SH7045 and SH7044, which have a large

*1: Registered trademark of Microsoft Corp.

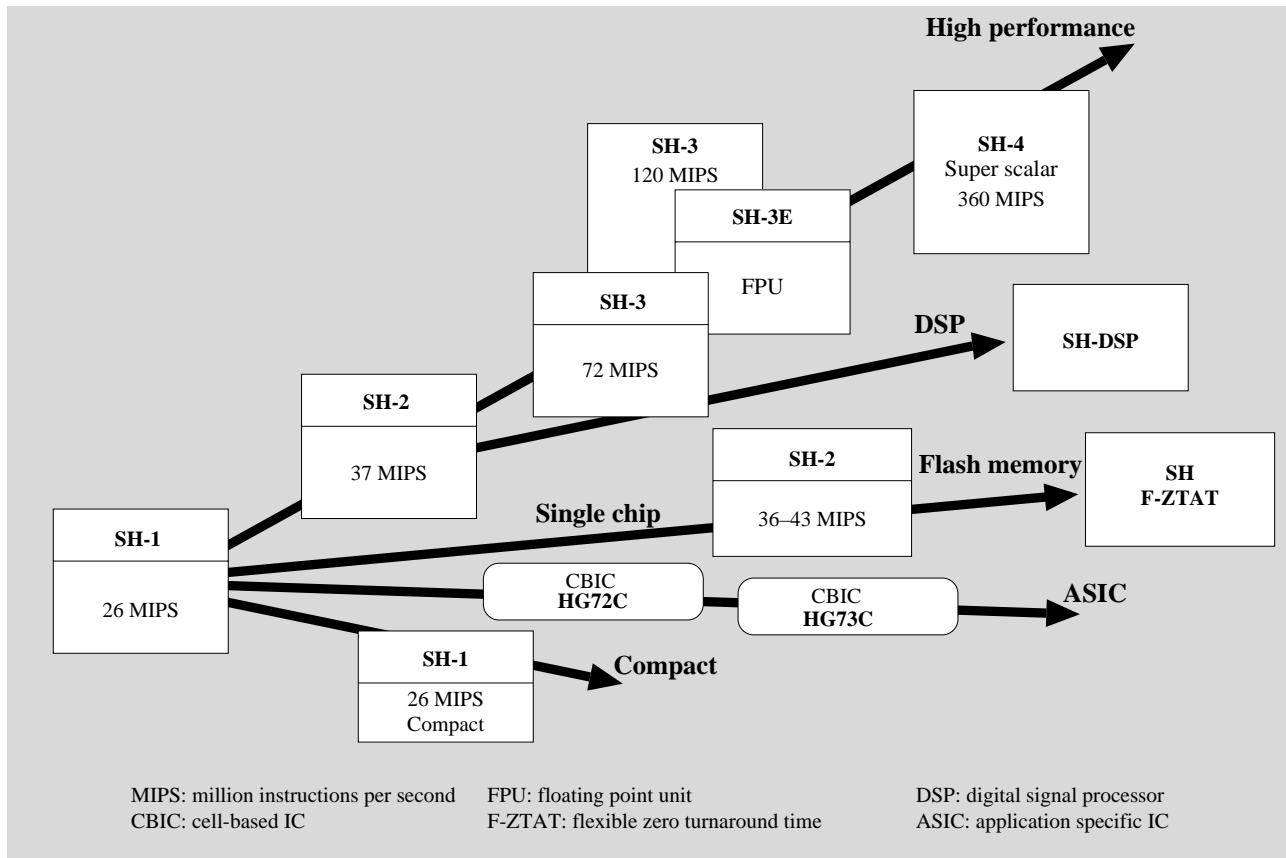


Fig. 1—SuperH RISC Engine Family Roadmap.

The SuperH RISC engine family is evolving in various directions such as high performance, flash memory on chip, and ASIC.

flash memory of 256 kbyte.

The third product, the SH-3 — including the SH7708, SH7707, and SH7709 — was developed for portable information instruments that need high performance, small size, and low power consumption. The reasons for widespread adoption of the SH-3 for Windows CE applications include: Windows CE can run on small storage size memory; a high MIPS/W; and HPCs can be built with a small number of parts. The SH's 16-bit fixed length instruction code can decrease the memory size to 2/3 that of other RISC architecture's 32-bit length instruction code because of its good code efficiency. The SH-3 can implement an HPC with small memory size; namely 4-Mbyte of ROM and 2-Mbyte of RAM. It achieves both high performance and low power consumption. Because the SH-3 has an onboard 8-kbyte cache memory, it can reduce memory accesses and reduce system power consumption.

The SH-DSP (SH7410) has DSP-class signal processing capability through the use of Harvard architecture and flexible DSP parallel operation even

though it is a RISC microprocessor. For example, it can execute JPEG (Joint Photographs Experts Group) processing three times faster than the same frequency SH-3. Hitachi will continue to develop higher performance microprocessors.

WINDOWS CE SYSTEM SOLUTION

Fig. 2 shows the system configuration of a Windows CE HPC. The HPC has familiar PC applications such as Pocket Word and Pocket Excel even though it is very small. Moreover, it is a portable device that can run for several tens of hours powered only by internal batteries. For these highly functional portable devices, the microprocessor must feature both low power consumption and high performance.

The screen of the HPC can be either monochrome or color. The LCD controller is recommended to support a color screen. There are the demands for a 4-Mbit/s high speed infrared communication function. Modem function is important because e-mail or Internet access is becoming popular on portable devices. Therefore, there is a trend to support the

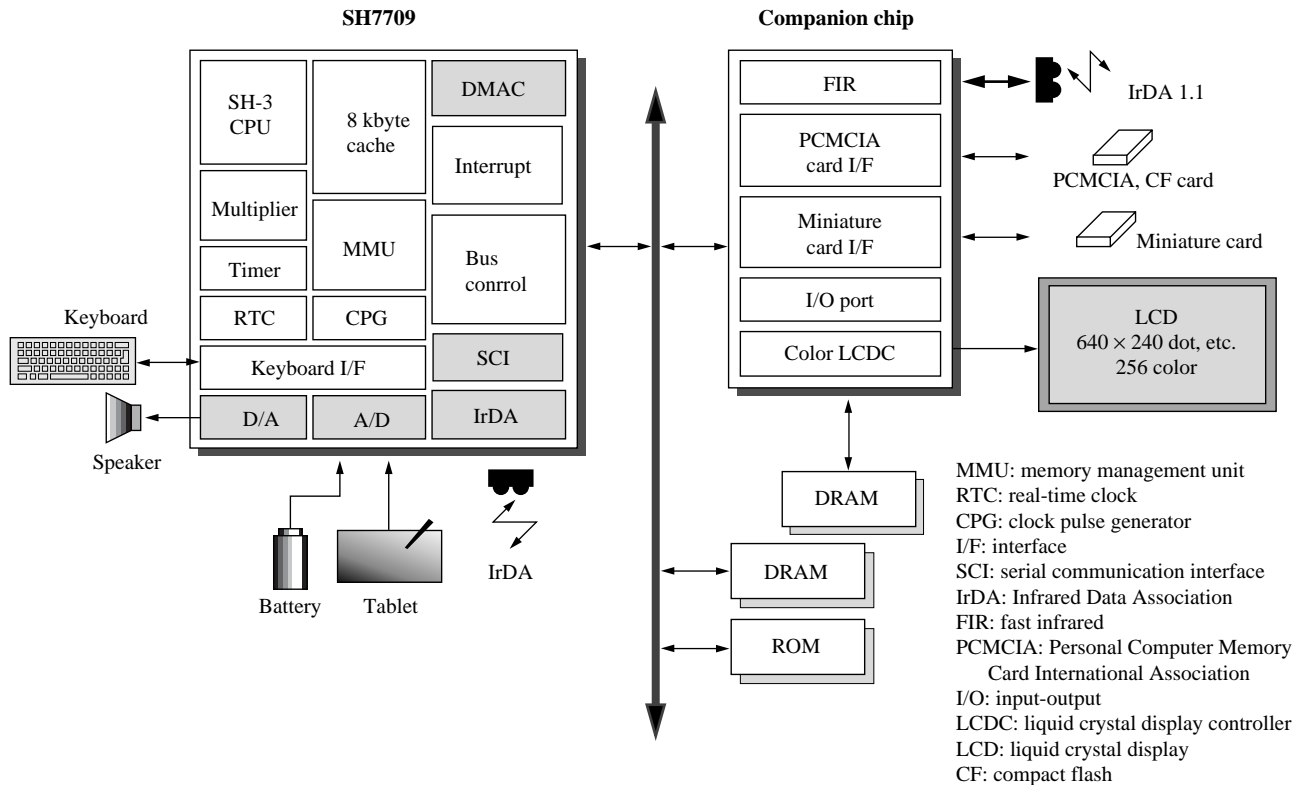


Fig. 2—Windows CE HPC System Configuration Example.
HPC system is configured from companion chip and SH7709.

modem function in software using the microprocessor. For other peripheral functions, a PCMCIA (Personal Computer Memory Card International Association) controller is needed to connect a PC card or compact flash card.

In addition to reduced CPU operating power consumption, power management functions such as dynamic clock frequency change and clock supply control to each module are extremely important when powering an HPC with batteries. There is also strong demand for low power to the peripheral LSI. In order to realize a small size and lightweight HPC, small and light LSI package such as LQFP (low profile quad flat package) and chip size package (CSP) should be provided.

There are many essential requirements for an HPC and a high performance microprocessor is one of them. A system solution is needed that includes a peripheral LSI and middleware. Hitachi offers system solution. This paper describes the SH7709 and its peripheral LSI, the HD64461, as part of the system solution. Hitachi is developing middleware to realize the modem function, picture compression, etc., for a complete solution. However, middleware is not described in this paper.

DEVELOPMENT OF THE SH7709 FOR THE MOBILE COMPUTING DEVICES

Hitachi developed the SH7709, which is a member of the SH-3 family, with HPCs as a target application. In these mobile computing devices, high performance, low power, and high integration are required. The microprocessor must have embedded peripheral functions to realize small size, light weight, and low system power. SH7709 realized these requirements with the high performance of 96 MIPS, the low power consumption of 300 MIPS/W, and on-chip peripherals.

(1) High performance at low power

The SH7709 is compatible with other SH3 family devices. It can run at 80 MHz, and supports the dynamic clock changing mechanism, module standby function, sleep function and standby function incorporated in other SH-3 family devices. It also supports a X3 clock mode and dynamic power management of each arithmetic unit, enabling it to achieve the high power to performance ratio of 300 MIPS/W. The clock is supplied only to the arithmetic unit needed to execute the current instruction.

(2) Abundant functions

Fig. 3 shows the block diagram of SH7709. The CPU core area is compatible with the SH-3 series, there

GPIO: general purpose I/O port
 FIFO: first in, first out
 MMU: memory management unit
 DMAC: direct memory access controller
 RTC: real time clock
 CPG: clock pulse generator
 SCI: serial communication interface

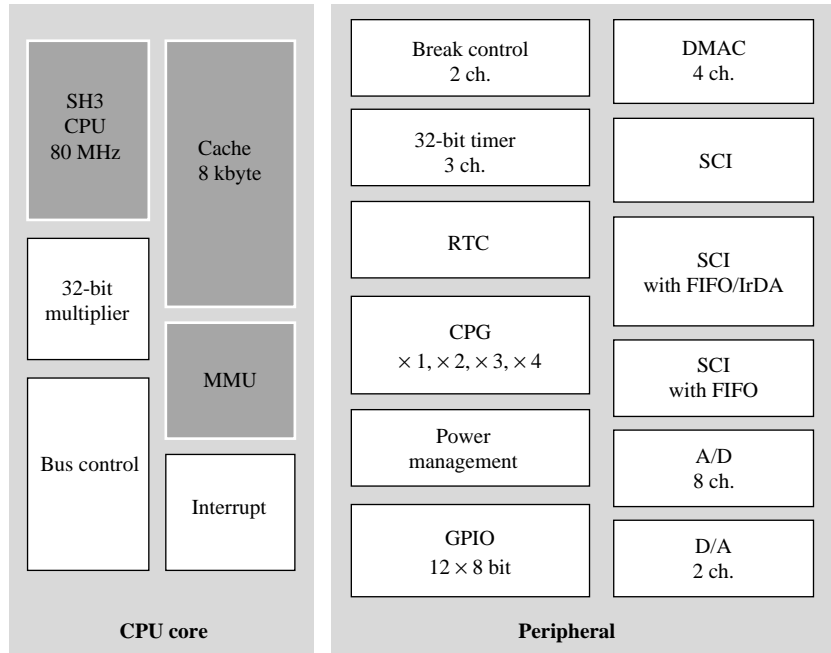


Fig. 3—SH7709 Block Diagram.
 The SH7709 includes various peripherals that are required for HPCs.

is an embedded 8-kbyte cache, and the direct memory interface supports the PCMCIA card and many types of memory including ROM, EDO (extended data output)-DRAM, and synchronous DRAM.

There are also many other peripherals on chip. There are 4 channels of DMAC, 8 channels of 10-bit A/D and 2 channels of 8-bit D/A for sound and touch panel, 3 channels of SCI, 3 channels of timer, RTC, and 12 eight-bit I/O ports. Two SCI channels out of 3 have 16-byte FIFO, and 1 channel out of 2 channels supports the IrDA1.0 (SIR) interface. To implement keyboard function, it supports restart from the standby mode by interrupt from the I/O port. The package is LQFP 208 pin and CSP 216 pin.

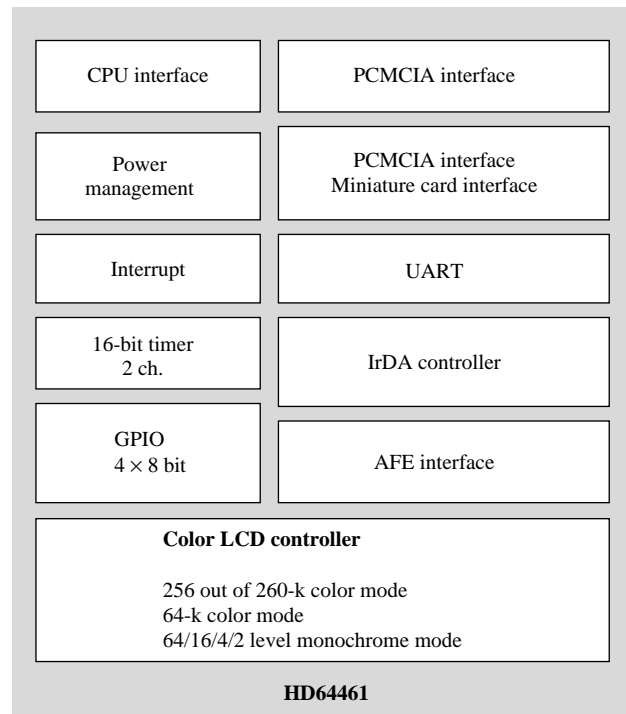
DEVELOPMENT OF THE SH-3/SH7709 CHIP SET, THE HD64461

The companion chip for the SH7709, the HD64461, was developed for the HPC. The HPC — which needs a small, high performance, and low power consumption companion chip — requires a system solution that includes peripheral functions. Thus the HD64461 incorporates various peripheral functions such as a color LCD controller and IrDA controller. It is possible to realize a small, high-performance, low-power consumption HPC with all logic in the HD64461 and SH7709.

(1) All needed functions on one chip

Fig. 4 shows the block diagram of HD64461. By

using the SH7709 as a host CPU, the HD64461 supports the Windows CE HPC. It has the color LCD controller, IrDA controller, RS232C controller, 2



UART: universal asynchronous receiver-transmitter
 AFE: analog front end
 GPIO: general purpose I/O port

Fig. 4—HD64461 Block Diagram.
 The HD64461 has peripherals necessary for HPC.

channels of PCMCIA controller, interface for the software modem and 2 channels 16-bit timer on one chip. It was developed with ITE Corporation. The color LCD controller supports a 640×240 pixel screen, and it can display 64-k colors or 256 colors out of 260-k colors. The IrDA controller supports 4-Mbps high speed communication in addition to 115.2 kbps. Furthermore, PCMCIA support is provided for two slots of PCMCIA, or for one slot for PCMCIA and the other slot for a compact flash card. The chip also has an analog front end (AFE) interface that can connect to an AFE LSI directly, so it can support data/fax modem by software modem. The package is LQFP 208 pin, and a CSP package is under development.

(2) Powerful power consumption control

To realize low power consumption, the HD64461 supports standby mode to each module. The user can select which modules are to be in standby mode. It can stop all modules including the clock by specifying standby mode to every module.

DEVELOPMENT TOOLS FOR HPC

The D9000 evaluation board has been developed to support development of the HPC with Windows CE.

Fig. 5 shows the system diagram of D9000. The D9000 supports Windows CE, and it has SH7708 as a CPU and FPGA for other peripheral circuits. The D9000 implements the functions of the HPC, and it has powerful debug facilities. Therefore, it is possible to debug the circuits and develop driver software for the peripheral circuits by using this evaluation board.

SUMMARY OF SUPERH MICROPROCESSOR, THE SH-4

The SH-4 was developed for assembly into multimedia devices such as next-generation mobile computing devices, set top boxes, and video game machines. Fig. 6 shows its highlights and structure. The SH-4 has a 32-bit floating point data matrix arithmetic unit that can process 3 dimensional graphics at high speed, and it can execute 4×4 matrix operation in 7 cycles. It supports superscalar architecture to execute two instructions in parallel. It has 8-kbyte instruction cache and 16-kbyte data cache.

The SH-4 achieves 360 MIPS at 200 MHz. In addition, the companion chip will be supplied as a component of a SH-4 chip set to build multimedia devices easily. This companion LSI will have not only

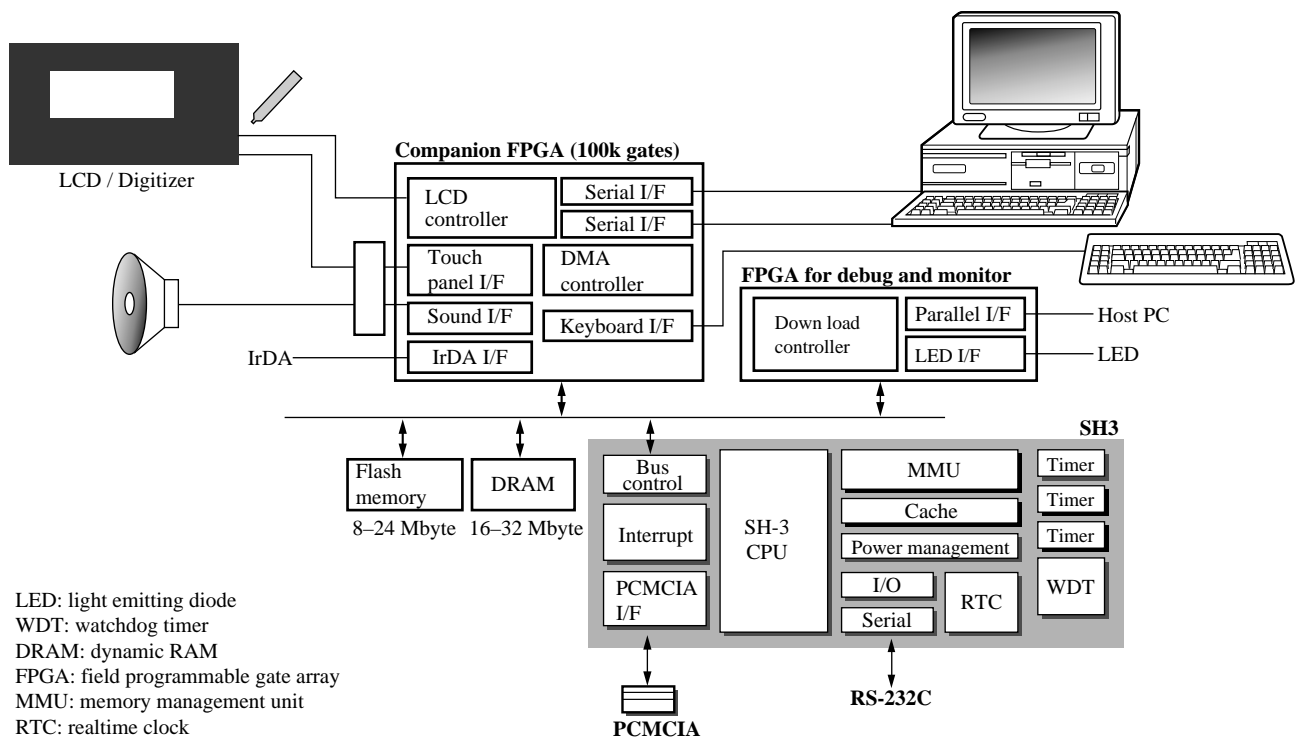
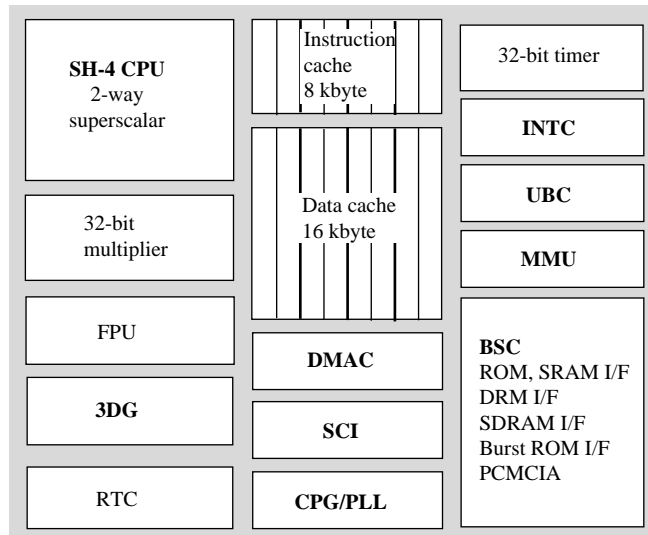


Fig. 5—D9000 Reference Platform System Diagram.

The D9000 reference platform can be used for circuit debugging and driver software development.

FPU: floating point unit
 3DG: three-dimensional graphics
 CPG/PLL: clock pulse generator/
 phase-locked loop
 INTC: interrupt controller
 UBC: user break controller
 BSC: bus state controller
 MMU: memory management unit



Features

Frequency 200 MHz
 Performance
 360 MIPS (Dhrystone)
 1.4 GFLOPS
 2-way superscalar
 Cache memory
 Instruction 8 kbyte,
 Data 16 kbyte
 Package 208 QFP
 256 BGA

Fig. 6—SH7750 (SH-4) Outline.
 The SH-4 achieves 360 MIPS at 200 MHz by its superscalar architecture, and separate instruction and data cache.

SH7750 (SH-4) block diagram

PCMCIA controller and IrDA controller but also interfaces for printer and universal serial bus (USB). The SH-4 was designed to support Windows CE, so Hitachi believes that it is possible to build a mobile computing device that has subnotebook PC level performance and functions with an SH-4 and its companion chip.

CONCLUSIONS

The HPC with Windows CE and other mobile computing devices require high performance and rich functions. Hitachi developed the SH7709 and HD64461 as a system solution for these devices. In the future, higher performance, lower power and richer functions will be required from these devices. Hitachi will continue to develop microprocessors and companion chips to meet these requirements. Hitachi will also develop software including middleware to offer system solutions.

REFERENCE

- (1) T. Baji et al., "SuperH and SuperH-DSP Microprocessors for the Mobile Computing Age," *Hitachi Review* **46**, No. 1 (Feb. 1997), pp. 3–8.

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