

# Evolution and Future of Critical Dimension Measurement System for Semiconductor Processes

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*OVERVIEW: Hitachi's first system for micro-scale dimensional measurement of semiconductors was the S-6000 CD-SEM commercialized in 1984 through a joint project between its electron microscope design and development division and semiconductor development division. Working on the concept of supplying a measurement system rather than just hardware, Hitachi undertook measurement system development in collaboration with users and research institutions from around the world. Hitachi has gained a reputation among users in recent years for measurement solutions as well as CD-SEMs and its products are used at nearly all leading LSI manufacturers, with the total number of units delivered to date due to exceed 4,000 units during 2011. Hitachi intends to continue helping users by supporting advances in semiconductors through measurement technology.*

## INTRODUCTION

EVEN in the era of VLSI (very-large-scale integration) technology, LSIs (large-scale integrated circuits) have continued to achieve higher levels of integration in accordance with Moore's Law<sup>(1)</sup>. The number of transistors per unit area in 2010 is more than one million times higher than in 1980, having continued to double every two years on average<sup>(2)</sup> and with further improvements in prospect.

In addition to progress in design technology, innovations in microfabrication have also contributed to these higher levels of integration by reducing minimum pattern dimensions by 70% every three years. CD-SEMs (critical dimension measurement scanning electron microscopes) are used in the semiconductor production process to measure properties of wafer circuit patterns such as line width and hole diameter. The measurement accuracy of these instruments has kept pace with advances in miniaturization since they first went on sale in 1984 and they have supported microfabrication of LSIs over this time by providing precise measurement techniques (see Fig. 1).

A Hitachi CD-SEM won the Okochi Memorial Production Prize in March 2008<sup>(3)</sup> in recognition of the contribution to LSI miniaturization made by its measurement technology and in June 2010 Dr. Hidehito Obayashi, Chairman of the Board [President, Chief Executive Officer and Director (then)] of Hitachi High-Technologies Corporation, the Hitachi

group company responsible for this business, received the IEEE Ernst Weber Engineering Leadership Recognition from the IEEE<sup>(4)</sup>.

This article describes how Hitachi's CD-SEMs have evolved in step with their users and the future prospects for this product.

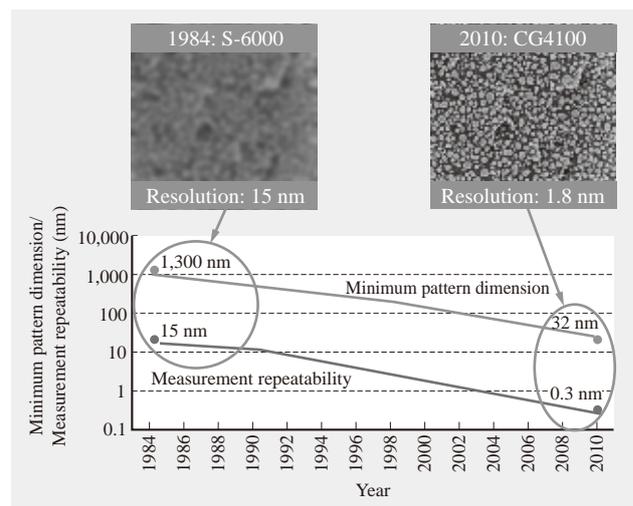


Fig. 1—Resolution and Measurement Repeatability Keeping Ahead of Finer Pattern Dimensions.

In response to finer pattern line widths (from 1,300 nm in 1984 to 32 nm in 2010), the resolution of CD-SEMs (critical dimension measurement scanning electron microscopes) has improved from 15 nm to 1.8 nm and measurement accuracy from 15 nm to 0.3 nm.

## DEVELOPMENTS AND ADVANCES IN CD-SEMS

### Transition from Scientific Device to Industrial Instrument<sup>(6)</sup>

In 1980, the industry was struggling to develop a process capable of achieving a minimum line width of 1  $\mu\text{m}$ . Steppers had a central role in microfabrication for the 1- $\mu\text{m}$  process but faced problems with CD (critical dimension) control<sup>(6)</sup>. There were also problems with measuring line widths using the optical techniques typically employed for dimensional measurement at this time.

Staff from Hitachi, Ltd.'s Semiconductor Business Division together with the device development center and the Central Research Laboratory which was working on semiconductor process development proposed using an electron microscope for dimensional measurement in place of optical techniques. They established a project in conjunction with the electron microscope development division and embarked on the development of a new system for measuring the dimensions of LSI patterns using electron beams. The concepts behind the development were as follows.

#### (1) Dedicated machine for dimension measurement

Since the very first model, Hitachi CD-SEMs have been distinct from the electron microscopes of that time. They use in-lens detection systems which do not cast a pattern shadow that could affect the measurement, and measurement techniques were developed based on use of a fast and precise XY stage.

#### (2) Industrial instrument suitable for use at production sites

The primary aim was to perform non-invasive measurements that did not require preparatory steps. This led to the adoption of measurement techniques that used low-energy electron beams. The second priority was that the instrument could be installed in production sites and the third was that the instrument would not require a specialist operator and could be used by anyone without operator-to-operator variation in measurement results.

At a time when electron microscopes were located in special-purpose dark rooms<sup>(7)</sup>, the idea of making an instrument that "could be installed in production sites" bordered on defiance of common sense. However, Hitachi was a leader in the field of electron microscope development and had technology for high-intensity FE (field emission) electron guns which it had just commercialized<sup>(8)</sup>. The CD-SEM performed rapid scanning (television scanning) of an electron beam from a high-intensity FE electron gun and was able to

be used without a dark room thanks to its use of image memory which was ahead of its time.

The concept of producing an instrument that could be used by anyone was a major step away from the assumption that electron microscopes were scientific devices for use by researchers. The user representative on the project team identified the measurement procedures used in the semiconductor production process and a computer-controlled measuring system that anyone could use to perform measurements was devised by programming these procedures as recipes that could be selected from a screen.

#### (3) Measurement system

Turning an electron microscope into a measuring instrument requires that it be made into a system whose measurements can be calibrated to ensure traceability. As no dimensional calibration system for electron microscopes existed even at public institutes, Hitachi embarked on the development of a dimensional calibration system in parallel with the development of the CD-SEM<sup>(9)</sup>.

In collaboration with the National Institute of Advanced Industrial Science and Technology, Hitachi developed the world's first "standard microscale with a 240-nm pitch" for use as a sample for nanometer-order calibration of magnification. The standard was later certified by the Japan Quality Assurance Organization (JQA) and made commercially available.

A "standard microscale with a 100-nm pitch" was also subsequently developed and released to keep pace with LSI miniaturization<sup>(10)</sup> (see Fig. 2).

The first-generation S-6000 CD-SEM developed through this project involving in-house users was announced at SEMICON Japan and went on sale in late 1984<sup>(11), (12)</sup>.

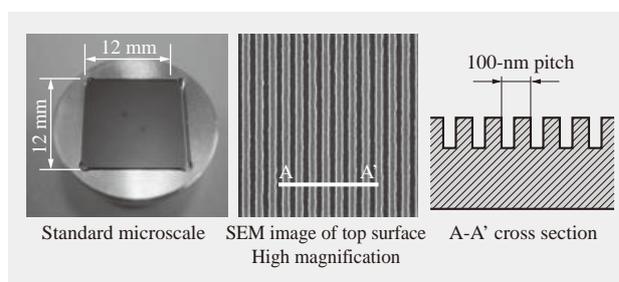


Fig. 2—Standard Microscale with a 100-nm Pitch for Calibration of Magnification.

This standard sample is used to calibrate the measurements of CD-SEMs. The sample is placed in the instrument to allow precise calibration of length measurement to be performed easily.

Model	S-6000	S-8820	S-9200	CG4000
Photograph				
Release date	1984	1994	1998	2006
Resolution (nm)	15	5	3	1.8
Repeatability (nm)	15	5	3	0.3
Throughput (wafers/h)	8 (manual operation) (6-inch wafer, 5-point measurement)	20 (automatic operation) (6-inch wafer, 5-point measurement)	45 (automatic operation) (8-inch wafer, 5-point measurement)	36 (automatic operation) (12-inch wafer, 20-point measurement)
Wafer size (inch)	4, 5, 6	5, 6, 8	6, 8	8, 12

Fig. 3—Evolution of CD-SEMs.

The CD-SEMs have earned a high reputation for stable operation in mass production environments and for the release of new models ahead of advances in semiconductor device miniaturization. Total deliveries to date are expected to surpass 4,000 during 2011.

### Evolution of CD-SEMs

The first-generation S-6000 model was adopted by semiconductor device manufacturers around the world and was followed by a series of models featuring enhancements based on user feedback. To date, Hitachi has developed the S-8000<sup>(13)</sup>, (14), (15), S-9000<sup>(16)</sup>, (17), and CG4000<sup>(18)</sup> Series (see Fig. 3).

The models in this product range also included modifications to suit changing times and user requests that are difficult to represent in terms of performance specifications. The S-8000 featured a fully revamped version of the FE electron gun that worked so well on the S-6000<sup>(5)</sup>. When requirements change with the times or at the request of users, the features that count as sales points also change drastically. Listening to users and satisfying their requests also increase the number of electron microscopes sold.

In addition to better repeatability, the S-9300 which went on sale in 1999 actively incorporated features based on user needs with an enhanced hole bottom observation function together with a revision of worldwide service arrangements. It was well received by users around the world for being ready in time for the shift to 300-mm wafers and for the comprehensive service arrangements.

### Productivity Improvement

Along with miniaturization, semiconductor devices are also subject to competition on cost reduction. Measurement instruments like CD-SEMs

	Item	Details
	Release date	2009
	Resolution	1.8 nm
	Repeatability	0.3 nm
	Throughput	42 wafers/h
	Wafer size	12 inches

Fig. 4—CG4100 CD-SEM and Main Specifications.

The CG4100 is a high-throughput instrument for 32-nm process production and 22-nm process development which was designed to meet the measurement needs of the latest generation of double patterning techniques.

are no exception and Hitachi has sought to improve performance factors such as uptime and throughput to satisfy users who are always looking to boost productivity.

The CG4000 which went on sale in 2006 met the requirements of its time and the latest CG4100<sup>(19)</sup> (see Fig. 4) which went on sale in 2009 resolved the problem of throughput in the charge sensitive layer step which has a high level of technical difficulty.

In this way, Hitachi's CD-SEMs have stuck to the concept of being an industrial instrument since the first S-6000 model, and over time development has continued to keep ahead of user requirements for repeatability and productivity. As a result, the CD-SEMs have won the trust of users not just for the high reliability and productivity<sup>(20)</sup> of individual instruments but also for the high uptime and extremely low tool-to-tool CD difference achieved when a number of instruments are operated on a production line<sup>(21)</sup>.

## MEASUREMENT APPLICATIONS

While high reliability is a prerequisite for measurement systems, user's concerns about measurement have changed over time. Hitachi's semiconductor measurement systems which mainly involve CD-SEMs have kept ahead of the times by developing and proposing measurement applications in conjunction with users in response to changing circumstances. The following sections describe typical measurement applications.

### Pattern Roughness Evaluation<sup>(18)</sup>

Since around 2003 when the microfabrication industry started development of the 90-nm process, a problem arose with reports of bumps of around 10 nm evident along the edges of patterns that are meant to be straight, a level of variation that is equal or larger than that permitted in dimensional control. Accordingly, a requirement specification for LER (line edge roughness) was added to the 2003 International Technology Roadmap for Semiconductors<sup>(2)</sup> (ITRS). The ITRS is a technology roadmap for the semiconductor industry created with the aim of improving LSI development efficiency and sponsored by industry bodies in Japan (Japan Electronics and Information Technology Industries Association), USA, Europe, South Korea, and Taiwan. The problem, however, was that different investigators reported different LER measurements and Hitachi was requested by manufacturers of devices, steppers, and resist to create and standardize a measurement procedure for LER.

In response, Hitachi in 2004 established a taskforce at Semiconductor Equipment and Materials

International<sup>(3)</sup> (SEMI), the industry's standards body, and developed technology for measuring LER<sup>(22)</sup> in collaboration with Japanese users, the National Institute of Standards and Technology<sup>(4)</sup> (NIST), the Semiconductor Manufacturing Technology Institute<sup>(5)</sup> (SEMATECH), the International SEMATECH Manufacturing Initiative<sup>(6)</sup> (ISMI) (an international semiconductor consortium that undertakes development jointly with SEMATECH), and ITRS (see Fig. 5).

Hitachi's proposal was adopted by an international vote as a SEMI standard<sup>(23)</sup> in 2006 and the taskforce was disbanded.

As well as responding to user requirements, Hitachi believes that its technical leadership in this standardization work was also highly regarded.

### Use of CAD Design Data in Measurement<sup>(24), (25), (26)</sup>

OPC (optical proximity correction) uses diffraction of the light on the surface to perform shape correction<sup>(27)</sup> and becomes necessary as the LSI dimensions become smaller than the wavelength of light used for pattern formation (lithography). Because OPC performs correction on the CAD (computer-aided design) data, it is necessary to establish correction rules that are detailed and accurate. Hitachi developed the DesignGauge solution system to collect the basic data needed to establish these rules. Precise correction by OPC becomes essential with greater levels of miniaturization and the time taken to produce the measurement recipes has also grown as the number of measurement points required to perform correction has jumped from a few thousand to several tens of thousands. In response, DesignGauge significantly improves the efficiency of recipe creation because it can produce measurement recipes quickly by performing the processing off-line before it is needed using the CAD data.

The number of correction locations and the size of corrections increase as LSI design rules get smaller and the time taken to create the correction rules has an impact on the LSI development time. DesignGauge has been jointly developed with a number of customers since it was a beta version and three of these customers<sup>(29), (30), (31)</sup> along with Hitachi<sup>(28)</sup> presented results from this work at the 2005 conference of the International Society for Optics and Photonics (SPIE) (shortly after DesignGauge was formally announced) which won acclaim. Fig. 6 shows a report excerpt.

Whereas dimension measurement had been adequate in the past, the higher precision of

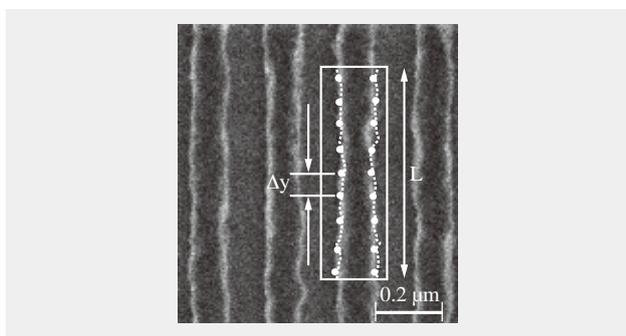


Fig. 5—Example LER (Line Edge Roughness) Measurement. Different types of resist were tested over a test area ( $L$ ) of  $2\ \mu\text{m}$  or more with an edge measurement pitch ( $\Delta y$ ) of  $10\ \text{nm}$  or less, these conditions being established as the SEMI (Semiconductor Equipment and Materials International) standard. A special function complying with this standard was developed for the CD-SEM to facilitate resist testing.

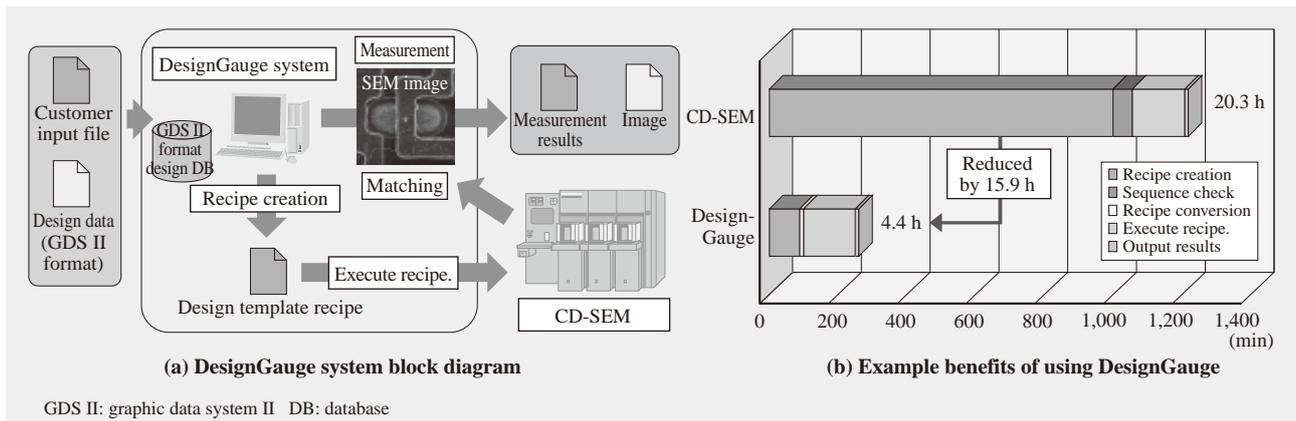


Fig. 6—DesignGauge System Block Diagram and Example Benefits.

Features of DesignGauge include improved OPC (optical proximity correction) evaluation accuracy, shorter work times, and the ability to produce recipes off-line without needing a CD-SEM or wafers. Installation of DesignGauge reduces the time for preparing recipes to about one-sixth of what was previously required.

OPC brought growing demand for more accurate measurement of pattern shapes such as line-ends and corners. In response, Hitachi, ahead of other companies, succeeded in significantly shortening development times by developing an automatic function to extract pattern feature lines from SEM images with high accuracy<sup>(32)</sup>.

DesignGauge is currently used by almost all leading LSI manufacturers and the software not only contributes to sales of CD-SEMs, it also adds to the value of Hitachi measurement systems, with Hitachi offering close support including biannual user meetings at SPIE in the USA and at SEMICON Japan, a trade show in Japan. Hitachi is continuing to take note of customer opinion and develop DesignGauge further and a family of complementary products is available consisting of RecipeDirector which enhances the recipe creation function and DG-Analyzer which enhances OPC evaluation<sup>(33)</sup>.

## FUTURE TECHNICAL ISSUES AND PROSPECTS

LSIs are becoming more complex and the levels of miniaturization are higher. In addition to joint development with key customers, Hitachi also participates in joint research and other activities with International Business Machines Corporation (IBM) and international consortiums such as the imec (Interuniversity Microelectronics Center) in the Kingdom of Belgium and SEMATECH in the USA. This provides opportunities to continue developing

Hitachi's semiconductor measurement systems in anticipation of user needs.

Double patterning is currently being adopted to achieve smaller pattern sizes. Although the issues with this method include not only measurement and control of pattern dimensions but also of the very small pattern overlay error in the chips, Hitachi has kept ahead of the times by working with customers to develop fine-scale overlay measurement technology using CD-SEMs<sup>(34), (35)</sup>.

Resist LER is one of the challenges in commercializing EUV (extreme ultraviolet) lithography, a leading contender for providing the next generation of microfabrication technology, and measurement and control of LER will become increasingly important in future. Hitachi's measurement systems will provide measurement technology to support the commercialization of EUV lithography.

The use of more complex structures has led to demand for ways of monitoring the 3D (three-dimensional) shape of micro-features. Hitachi is developing an entirely new measurement concept for its measurement systems that can accurately monitor 3D shapes using measurements from above<sup>(25), (36), (37)</sup>.

Meanwhile, in the area of productivity improvement, Hitachi also continues to work on developments and enhancements with a range of different approaches including automatic recipe generation from design data, higher throughput, and smaller tool-to-tool CD differences.

## CONCLUSIONS

This article has described how Hitachi's CD-SEMs have evolved in step with their users and the future

\* GDS II is a standard format for LSI layout design data. It was developed by Calma, Co. of the USA and, following acquisition by a series of other companies, it is currently the intellectual property of Cadence Design Systems, Inc. of the USA.

prospects for this product.

In 2010, Hitachi celebrated 25 years of involvement with systems for performing fine-scale measurement of semiconductors which dates back to the initial S-6000 CD-SEM. In that time, Hitachi has gained more than 80% of the global market and expects to deliver its 4,000th machine during 2011.

Hitachi intends to satisfy the expectations of users around the world by making further advances in measurement systems for semiconductors to help provide greater value for customers while also adding value to the Hitachi brand.

## REFERENCES

- (1) G. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, **38**, No. 8, April 19 (1965).
- (2) ITRS, "2009 ITRS Product Technology Trends," Executive Summary, p. 72, ITRS (2009).
- (3) "'Okochi Memorial Production Prize' for Critical Dimension SEM's Contribution to Semiconductor Scaling," *Hitachi Technology 2009–2010*, p. 28 (Aug. 2009).
- (4) "Chairman of the Board Hidehito Obayashi, Hitachi High-Technologies Receives the IEEE Ernst Weber Engineering Leadership Recognition Award," *Hitachi Technology 2011–2012*, p. 48 (Jul. 2011).
- (5) H. Obayashi, "Advances in Electron Microscopy that Support Innovation—Paradigm Shift from Leading-edge Scientific Analysis Device to Industrial Measuring Instrument," *Hitachi Hyoron* **91**, pp. 806–811 (Nov. 2009) in Japanese.
- (6) F. Dill, "Optical Lithography," *IEEE Trans. Electron Devices* ED-22, 440–444 (1975).
- (7) "Principles and Applications of Scanning Electron Microscopes," Japanese Society of Electron Microscopy, Kanto Region, Kyoritsu Shuppan Co., Ltd. (1983) in Japanese.
- (8) "Development of High-performance Electron Microscope," *Hitachi Hyoron* **64**, p. 69 (Jan. 1982) in Japanese.
- (9) Y. Nakayama et al., "Proposal for a New Submicron Dimension Reference for an Electron Beam Metrology System," pp. 1930–1933, *J. Vac. Sci. Technol. B*, No. 6, Nov/Dec (1988).
- (10) Y. Nakayama et al., "Sub-50-nm Pitch Size Grating Reference for CD-SEM Magnification Calibration," *Proc. SPIE* **7272**, 727224 (2009).
- (11) "Development of S-6000 Scanning Electron Microscope for Semiconductor Critical Dimension Measurement," *Hitachi Hyoron* **67**, p. 77 (Jan. 1985) in Japanese.
- (12) T. Otaka et al., "Evaluation Equipment for Semiconductor Process," *Hitachi Hyoron* **68**, pp. 725–730 (Sep. 1986) in Japanese.
- (13) "High-resolution Critical Dimension Measurement Electron Microscope," *Hitachi Hyoron* **77**, p. 58 (Jan. 1995) in Japanese.
- (14) T. Otaka et al., "Evaluation Equipment for Semiconductor Process Using Electron Beam," *Hitachi Hyoron* **77**, pp. 795–800 (Nov. 1995) in Japanese.
- (15) T. Otaka et al., "High-resolution Electron Beam Length Measuring Equipment," *Hitachi Hyoron* **79**, pp. 815–820 (Oct. 1997) in Japanese.
- (16) O. Nasu et al., "New CD-SEM System for Sub-10 nm Process Generation," *Hitachi Hyoron* **84**, pp. 267–270 (Mar. 2002) in Japanese.
- (17) H. Kawada et al., "CD-SEM for 65 nm Process Node," *Hitachi Hyoron* **85**, pp. 311–316 (Apr. 2003) in Japanese.
- (18) A. Yamaguchi et al., "CD-SEM Technologies for 65-nm Process Node," *Hitachi Review* **54**, pp. 15–21 (Jan. 2005).
- (19) H. Okano et al., "Views on Use of CD-SEMs as Production Management Machines," *Proceedings of 64th Conference of The Japanese Society of Microscopy*, p.38, MG03-01 (May 2008) in Japanese.
- (20) "CG4100 High-resolution CD-SEM," *Hitachi Hyoron* **93**, p. 104 (Jan. 2011) in Japanese.
- (21) H. Abe et al., "CD-SEM Tool Stability and Tool-to-tool Matching Management Using Image Sharpness Monitor," *Proc. SPIE* **7272** 727210-1 (2009).
- (22) A. Yamaguchi et al., "Characterization of Line-edge Roughness in Resist Patterns and Estimations of its Effect on Device Performance," *Proc. SPIE* **5038**, pp. 689–698 (2003).
- (23) SEMI Standard P47-0307, "Test Method for Evaluation of Line-Edge Roughness and Linewidth Roughness."
- (24) I. Kawata et al., "Critical Dimension-Scanning Electron Microscope 'CG4000' and DesignGauge System for Utilizing Design Data for Enhancing Yield of Next-generation Devices," *Hitachi Hyoron* **89**, pp. 336–341 (Apr. 2007) in Japanese.
- (25) I. Kawata et al., "New World of CD-SEM in Utilization of Design Data," *Hitachi Review* **55**, pp. 61–67 (Jun. 2006).
- (26) S. Koshihara et al., "Challenge to New Metrology World by CD-SEM and Design," *Hitachi Review* **57**, pp. 123–126 (Jun. 2008).
- (27) S. Hotta et al., "Layout Design and Lithography Technology for Advanced Devices," *Hitachi Hyoron* **90**, pp. 332–337 (Apr. 2008) in Japanese.
- (28) H. Morokuna et al., "A New Matching Engine between Design Layout and SEM Image of Semiconductor Device," *Proc. SPIE* **5252**, 546–558 (2005).
- (29) H. Yang et al., "OPC Accuracy Enhancement through Systematic OPC Calibration and Verification Methodology for Sub-100 nm Node," *Proc. SPIE* **5252**, 720–726 (2005).
- (30) P. Cantu et al., "Evaluation of Hitachi CAD to CD-SEM Metrology Package for OPC Model Tuning and Product Devices OPC Verification," *Proc. SPIE* **5252**, 1341–1352 (2005).
- (31) C. Tabery et al., "Use of Design Pattern Layout for Automatic Metrology Recipe Generation," *Proc. SPIE* **5252**, 1424–1434 (2005).
- (32) D. Hibino et al., "High-accuracy OPC-modeling by Using Advanced CD-SEM Based Contours in the Next-generation Lithography," *Proc. SPIE* **7638**, 76381X (2010).
- (33) "Design Solutions for Semiconductor Lithography," *Hitachi Hyoron* **92**, p. 91 (Jan. 2010) in Japanese.

- (34) S. Hotta et al., “Concerning the Influence of Pattern Symmetry on CD-SEM Local Overlay Measurements for Double Patterning of Complex Shapes,” Proc. SPIE **7638** 76381T (2010).
- (35) S. Hotta et al., “Spatial Signature in Local Overlay Measurements: What CD-SEM Can Tell Us and Optical Measurements Can Not,” Proc. SPIE **7638** 76381V (2010).
- (36) N. Yasui et al., “Application of Model-based Library Approach to Photoresist Pattern Shape Measurement in Advanced Lithography,” Proc. SPIE **7638** 763820 (2010).
- (37) T. Ishimoto et al., “Study on Practical Application to Pattern Top Resist Loss Measurement by CD-SEM for High NA Immersion Lithography,” Proc. SPIE **7638** 76382P (2010).

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